

Fig. 1

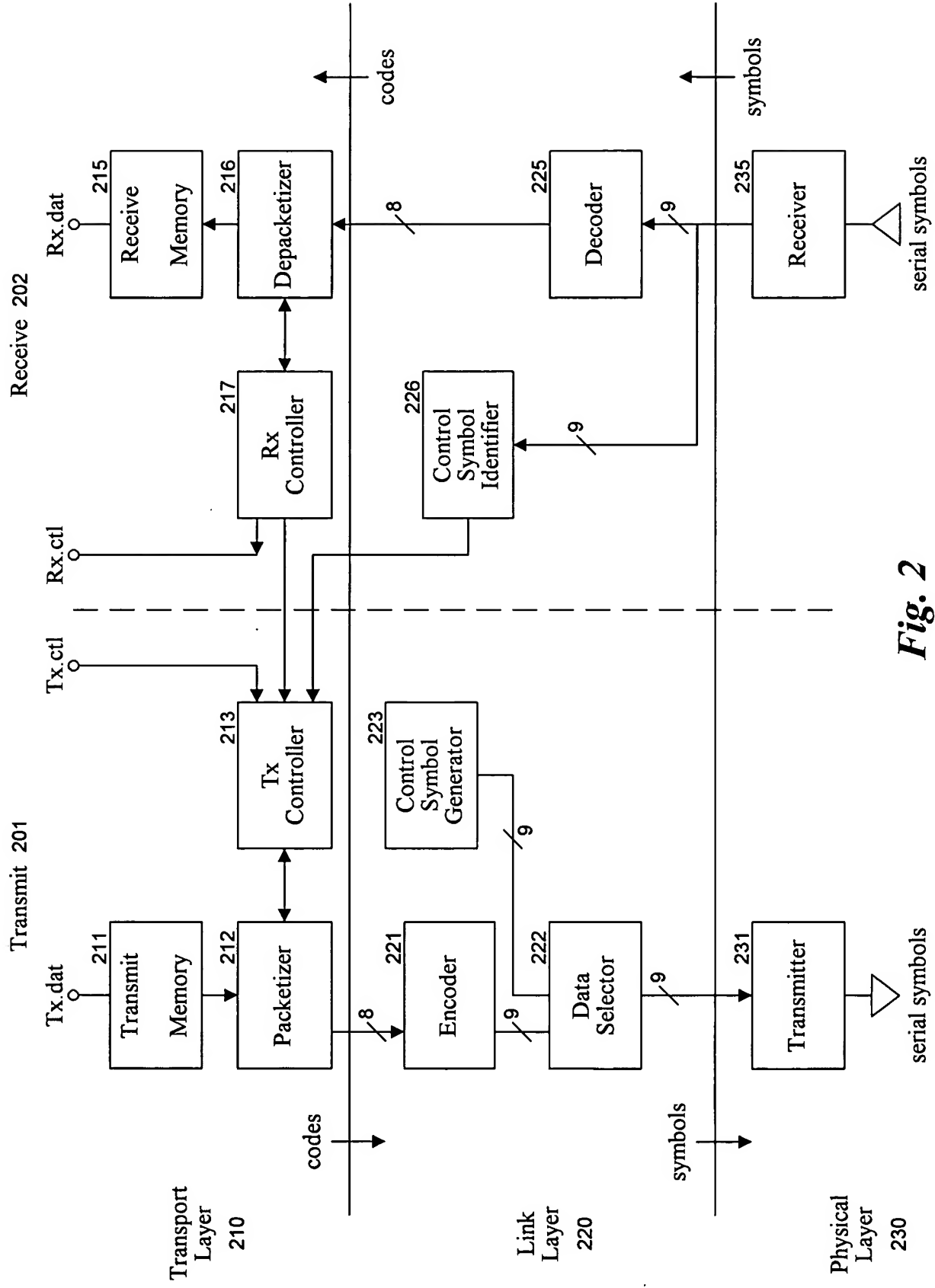


Fig. 2

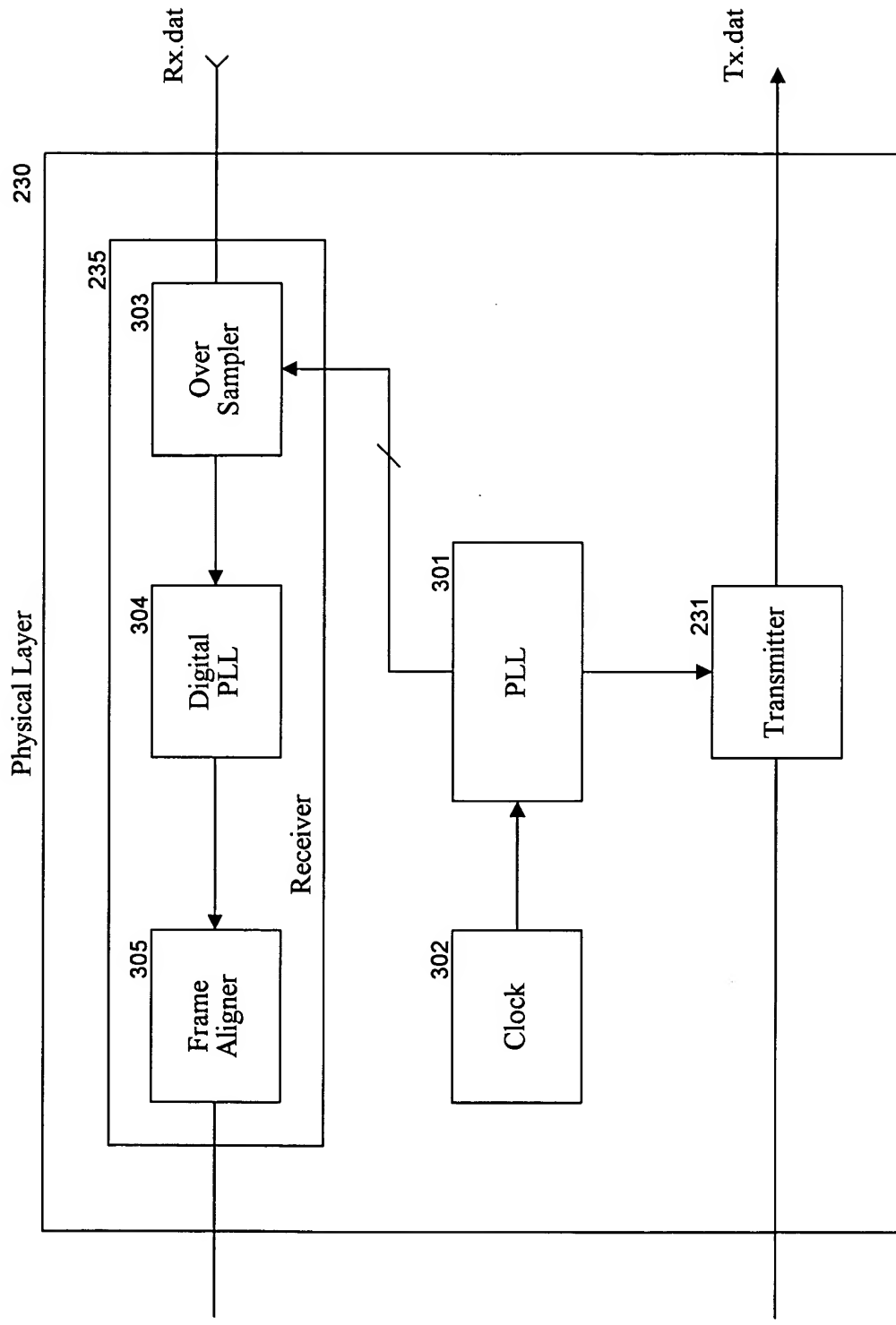


Fig. 3

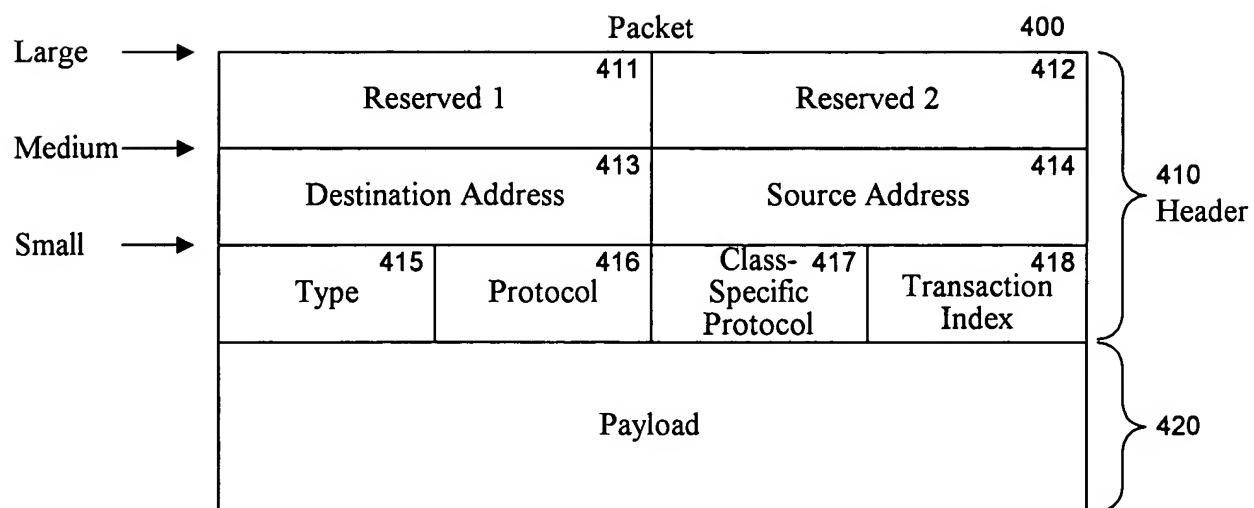


Fig. 4

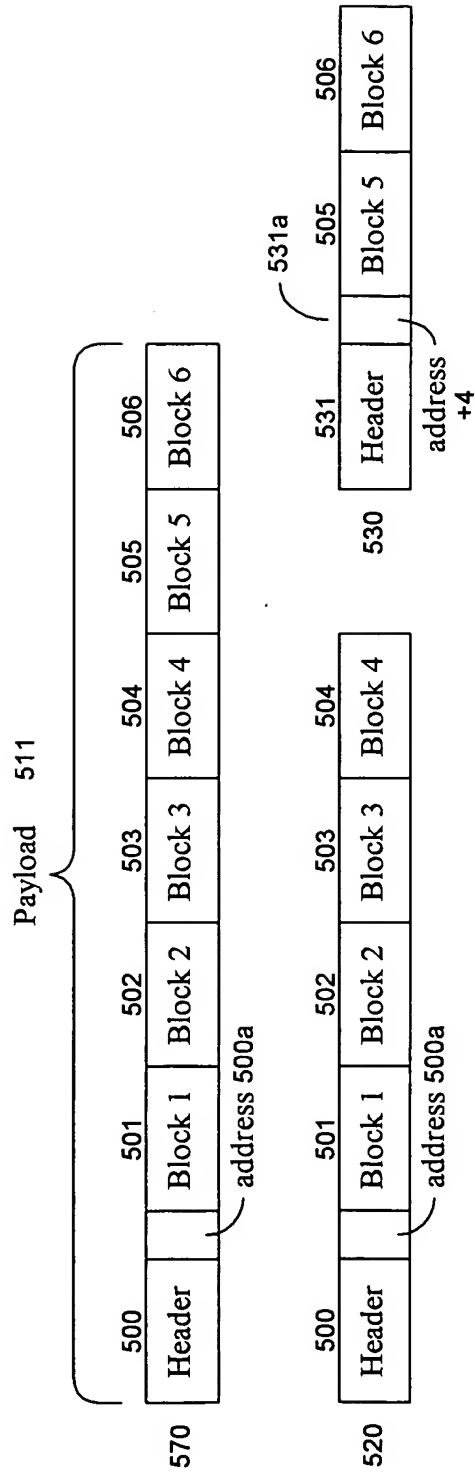


Fig. 5

FIG. 6

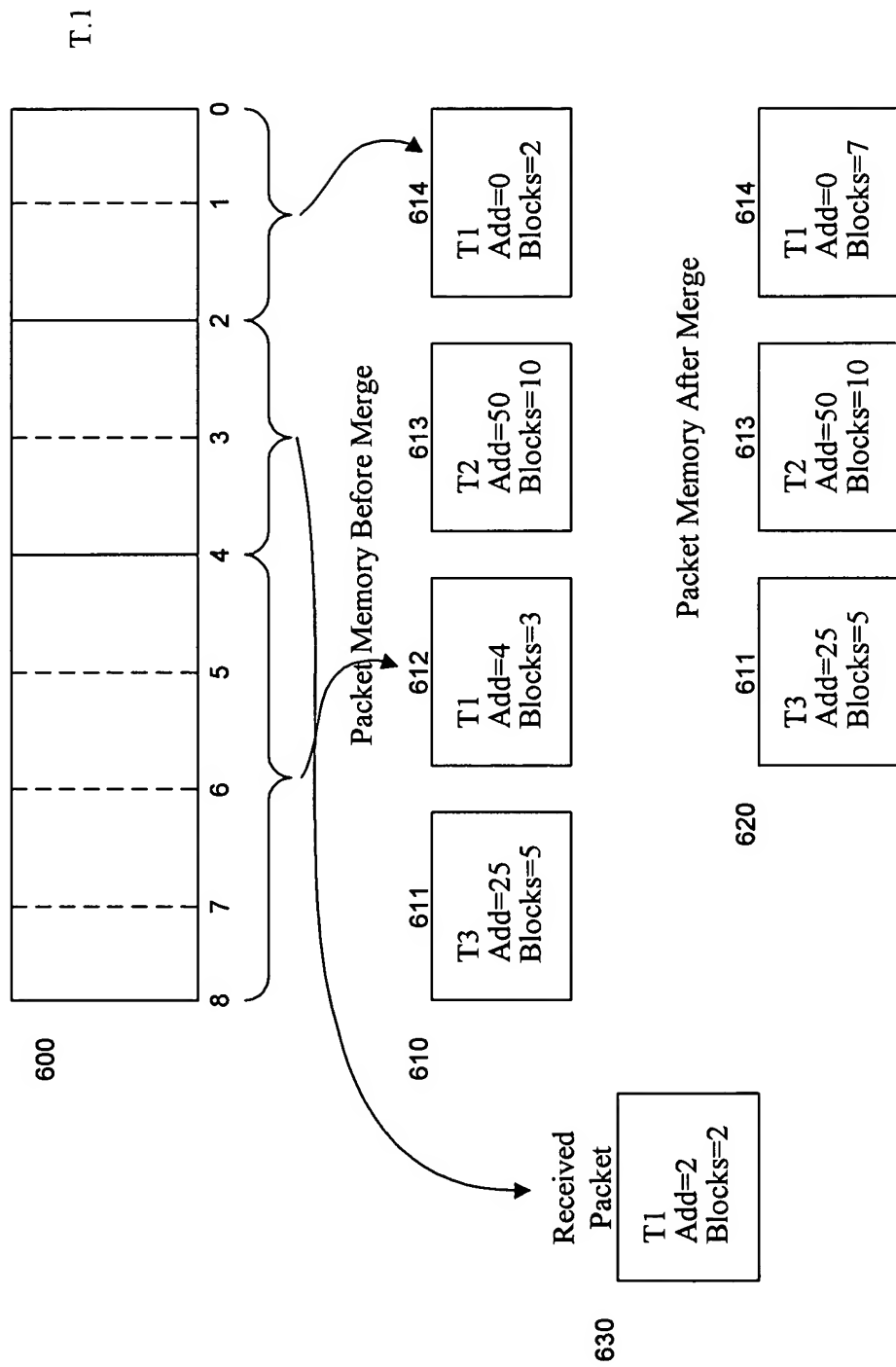


Fig. 6

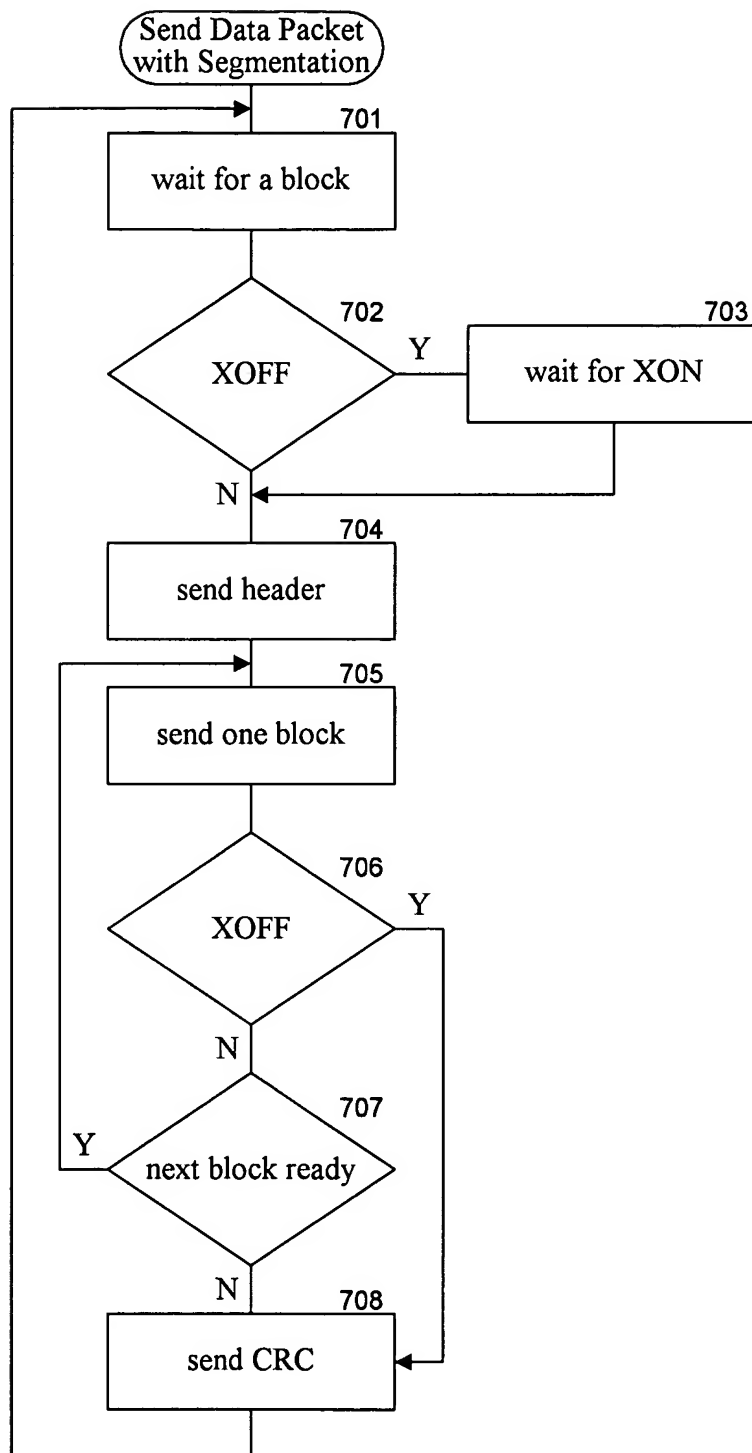


Fig. 7

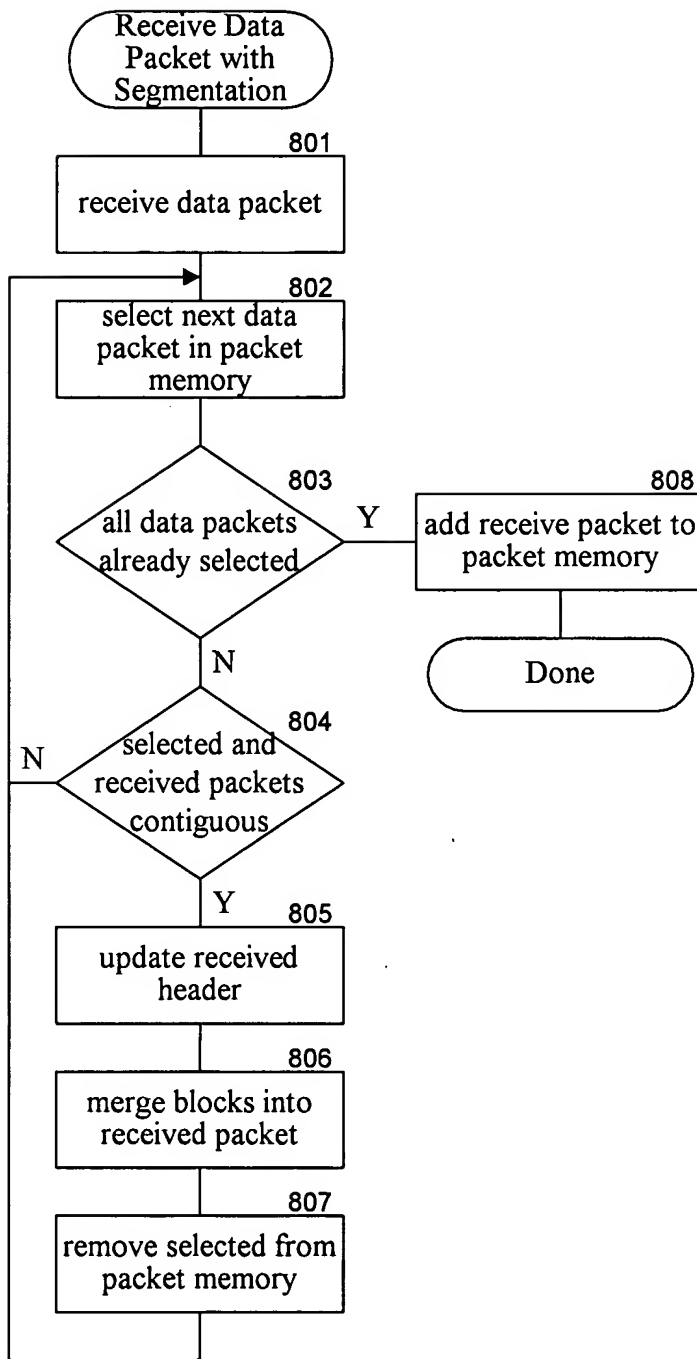
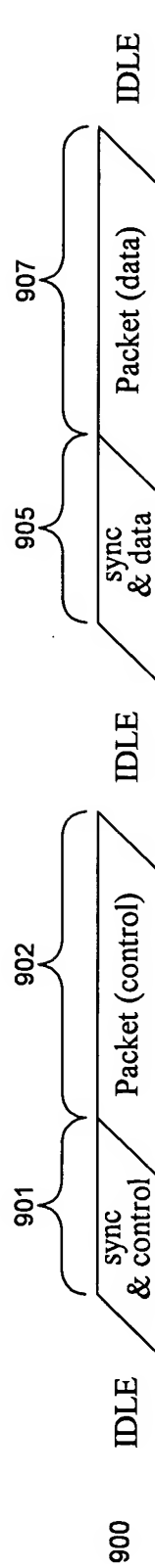


Fig. 8



sync & packet type

Fig. 9A

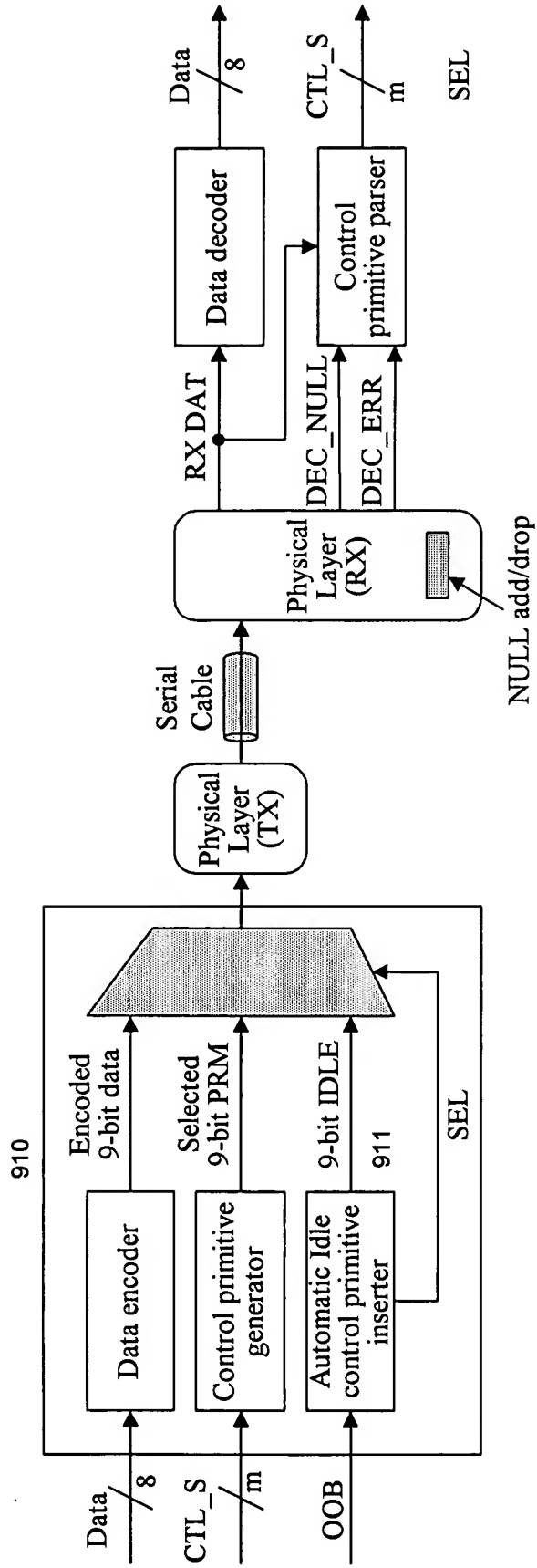


Fig. 9C

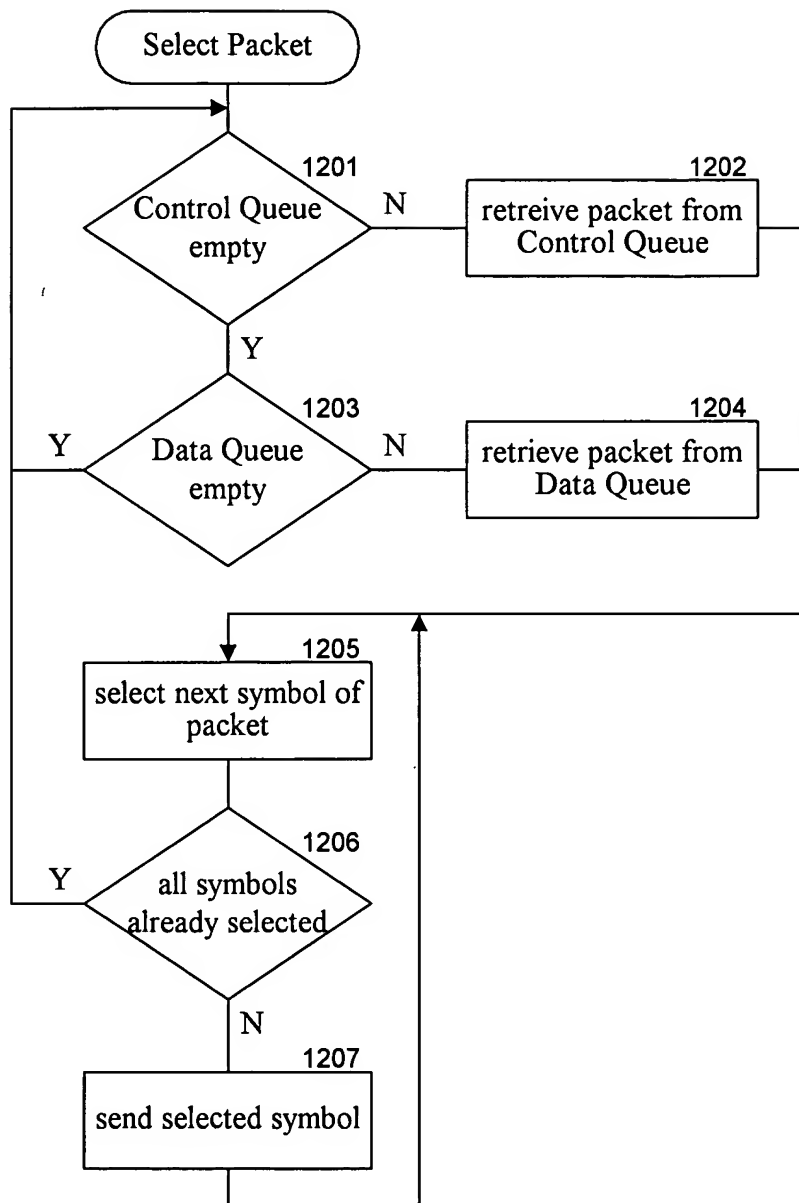


Fig. 12

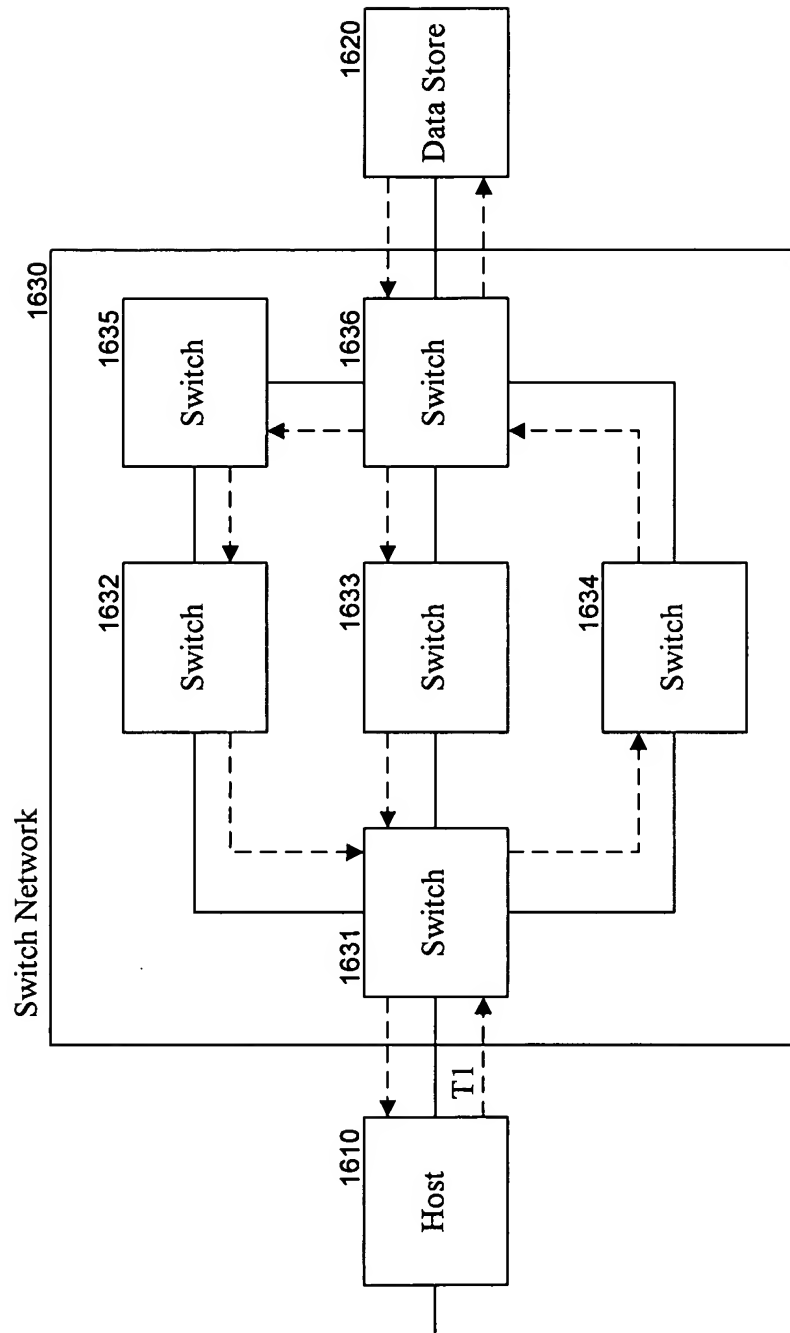


Fig. 16

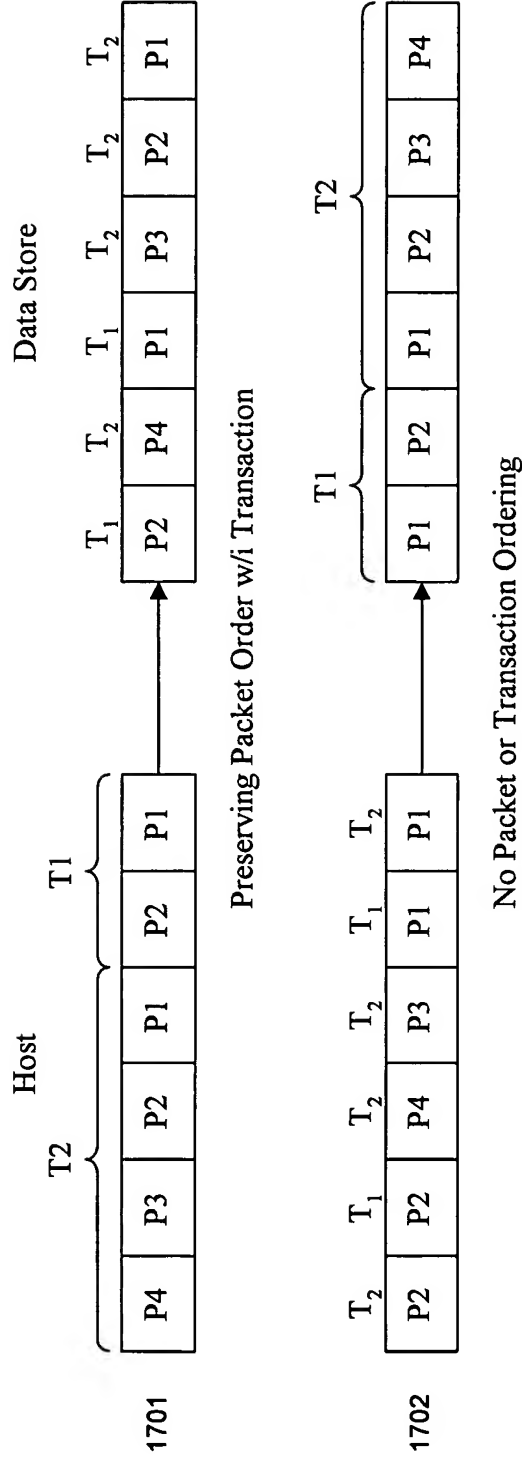


Fig. 17

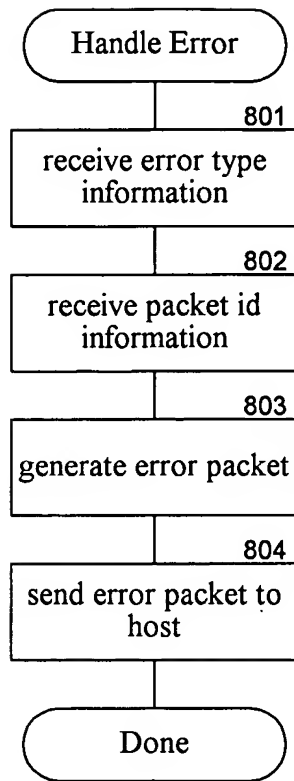


Fig. 19C

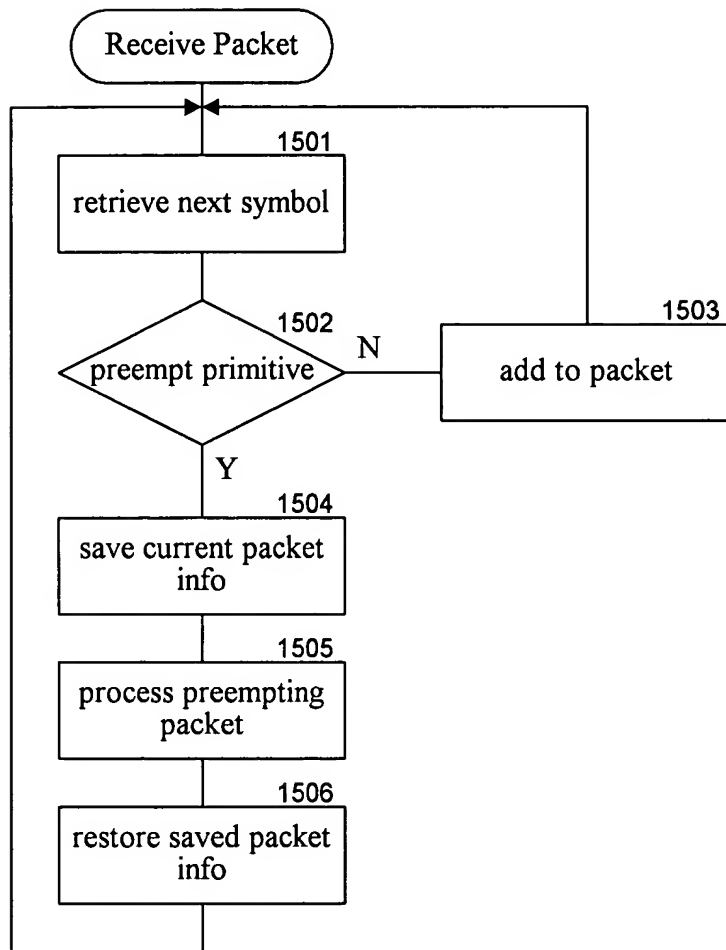


Fig. 15

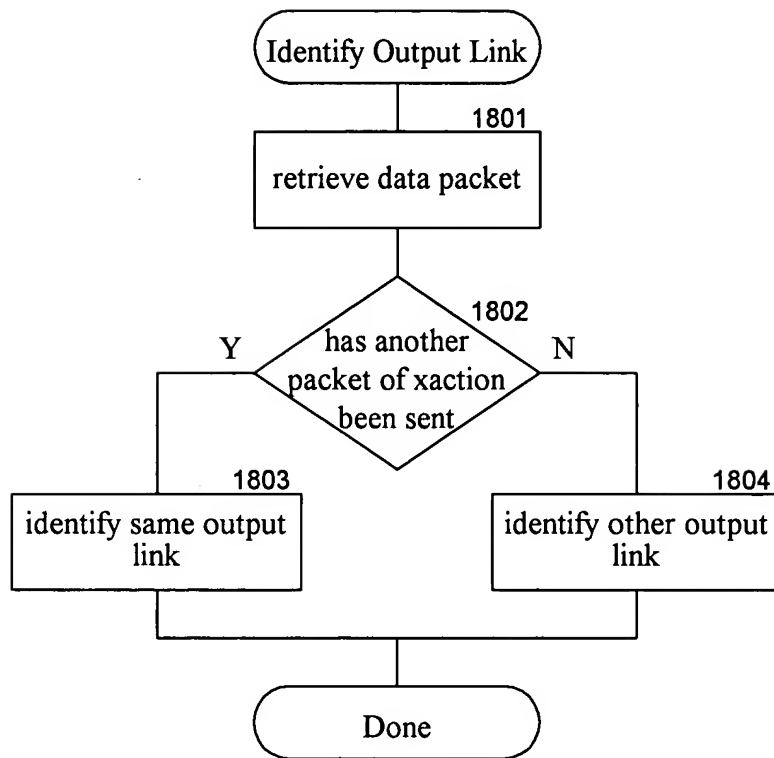


Fig. 18

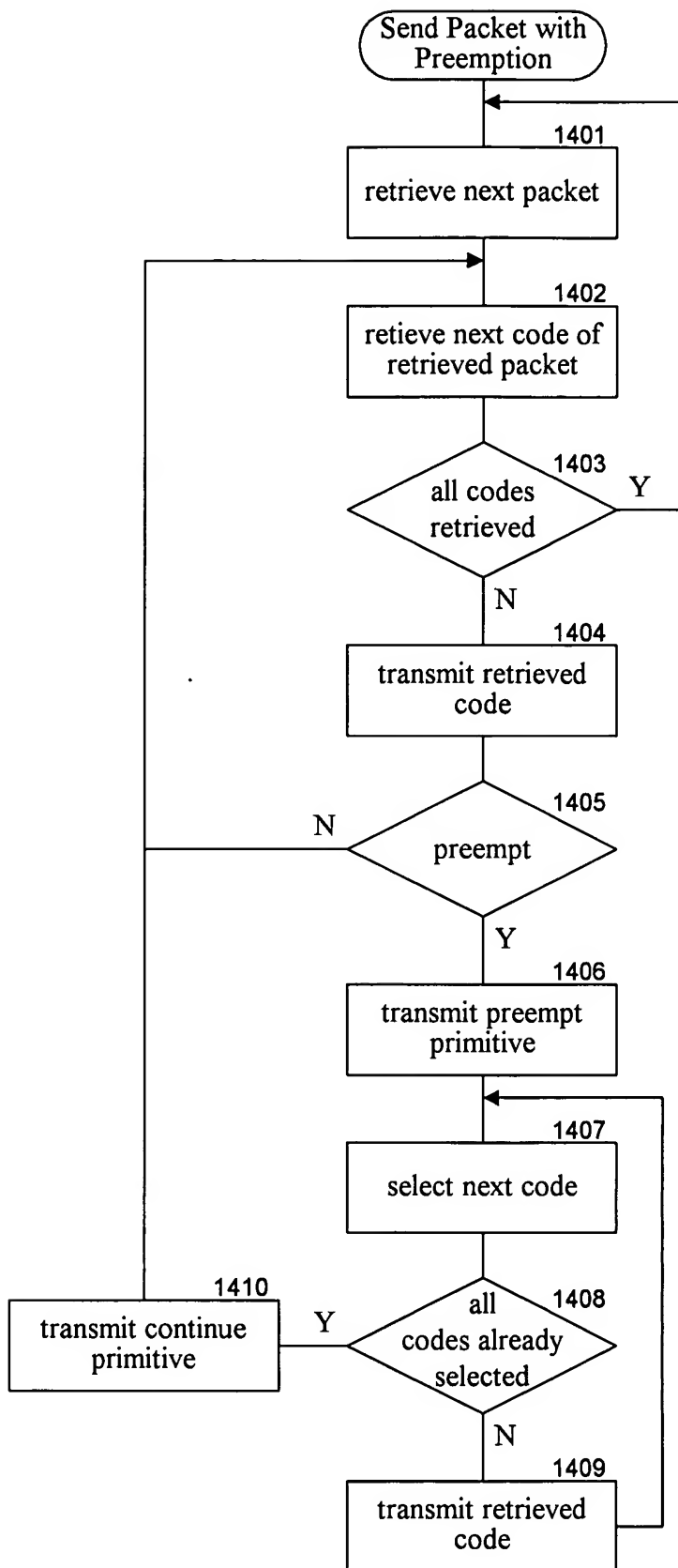


Fig. 14

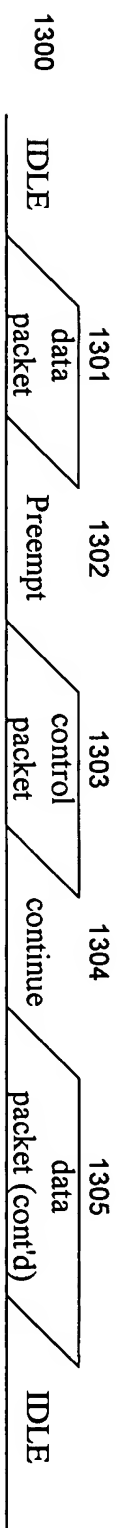


Fig. 13

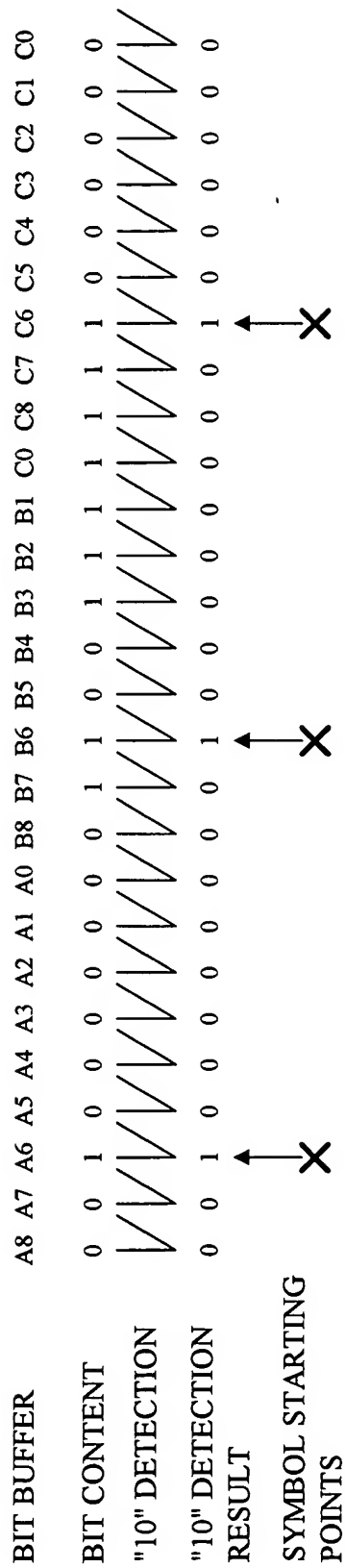


Fig. 9B

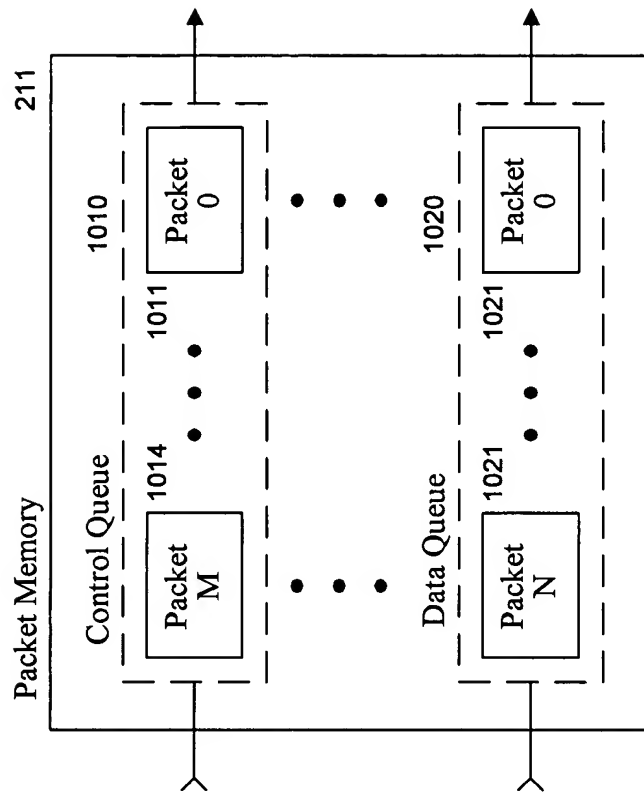


Fig. 10

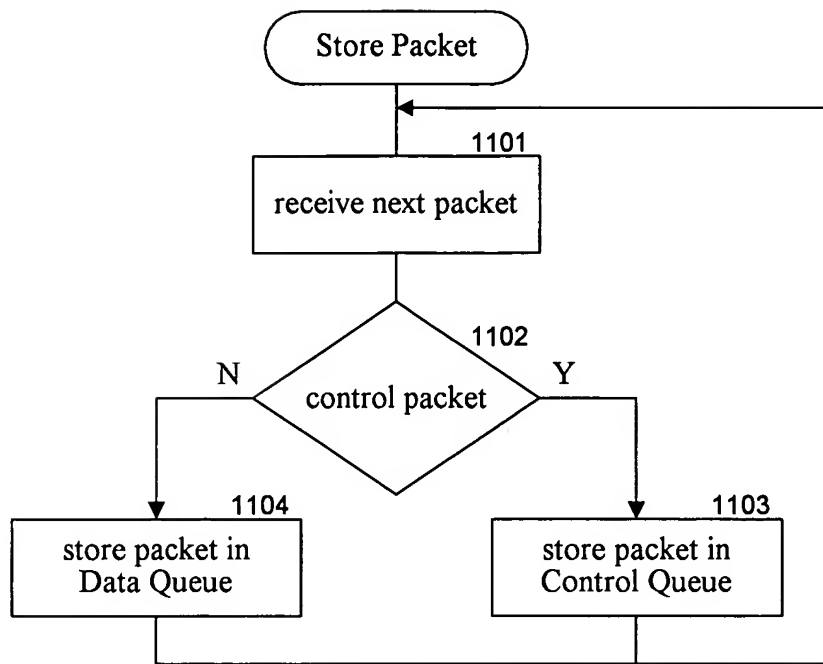


Fig. 11



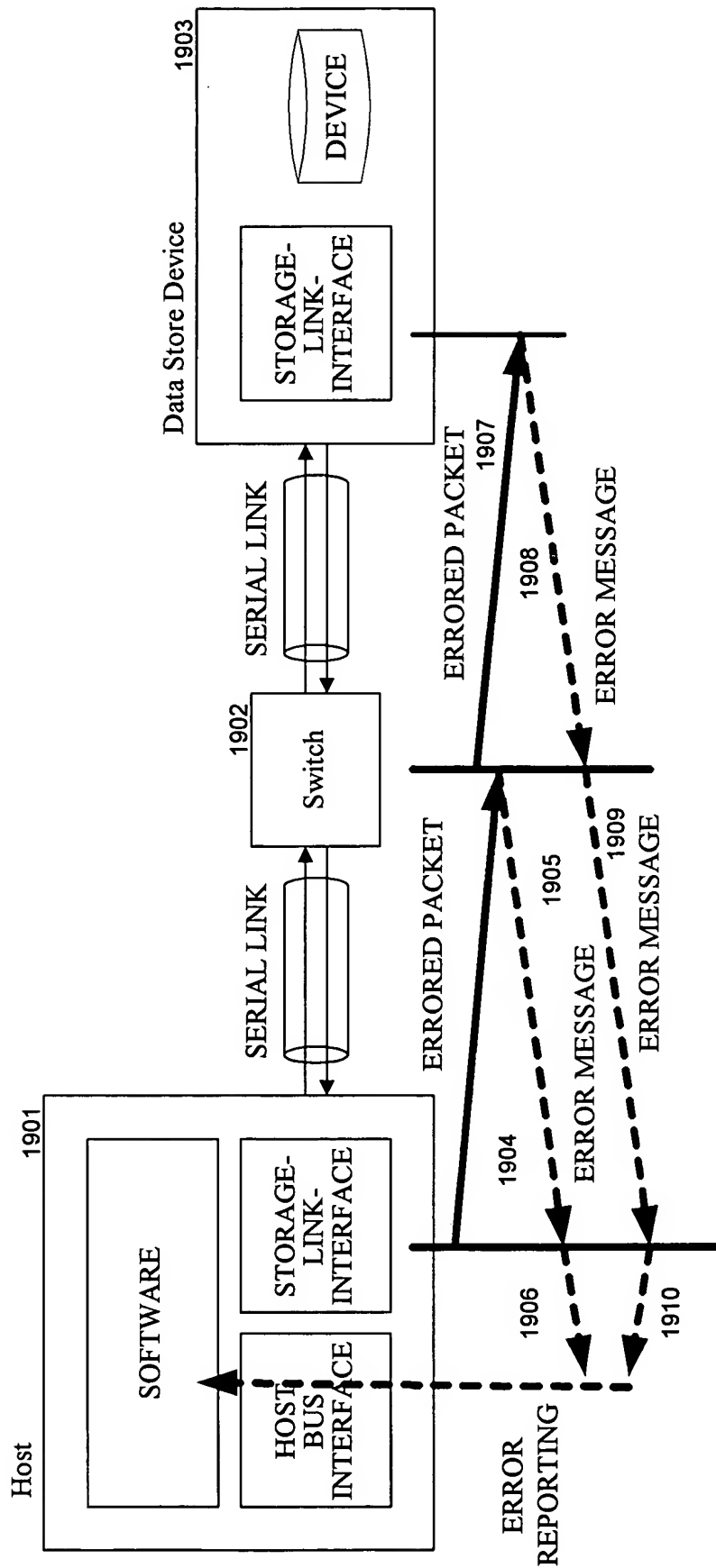


Fig. 19A

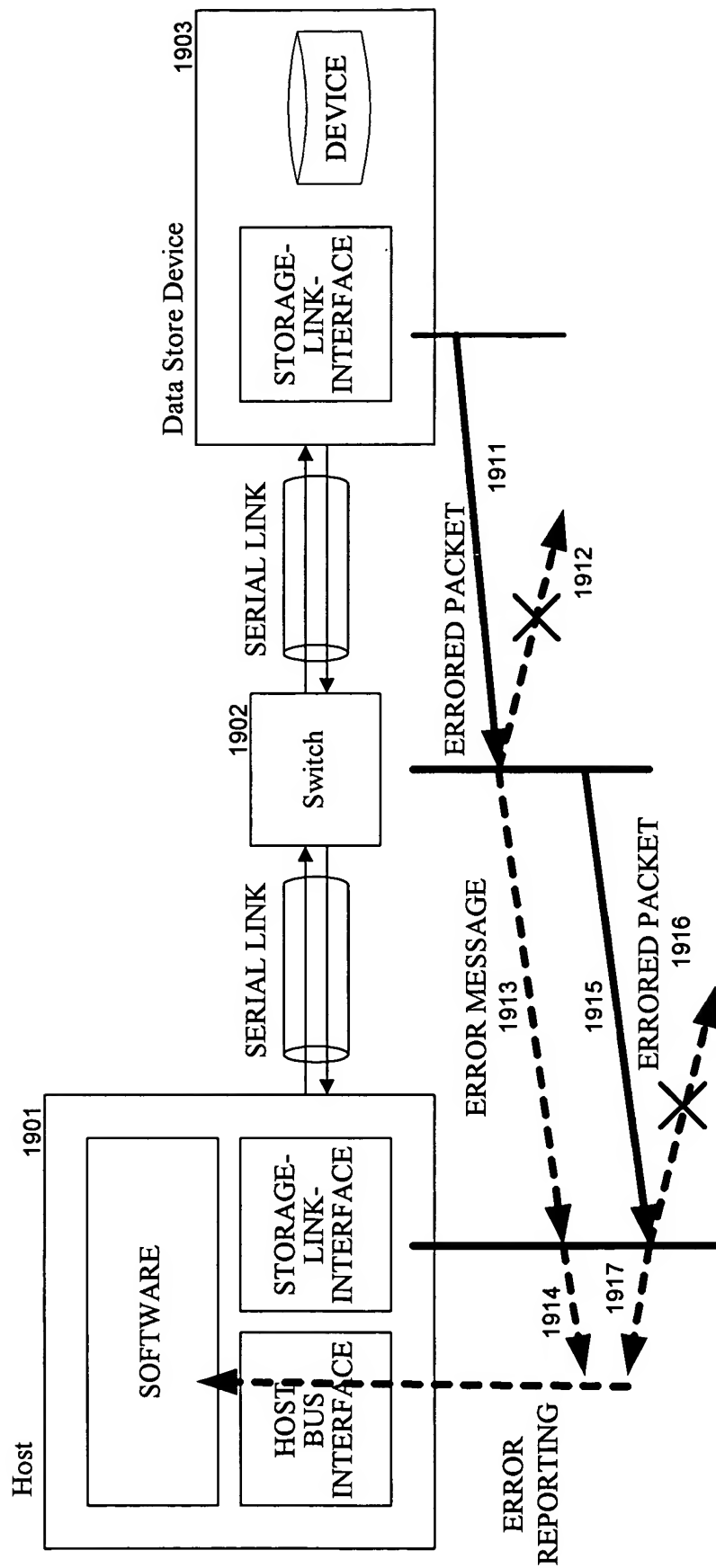


Fig. 19B

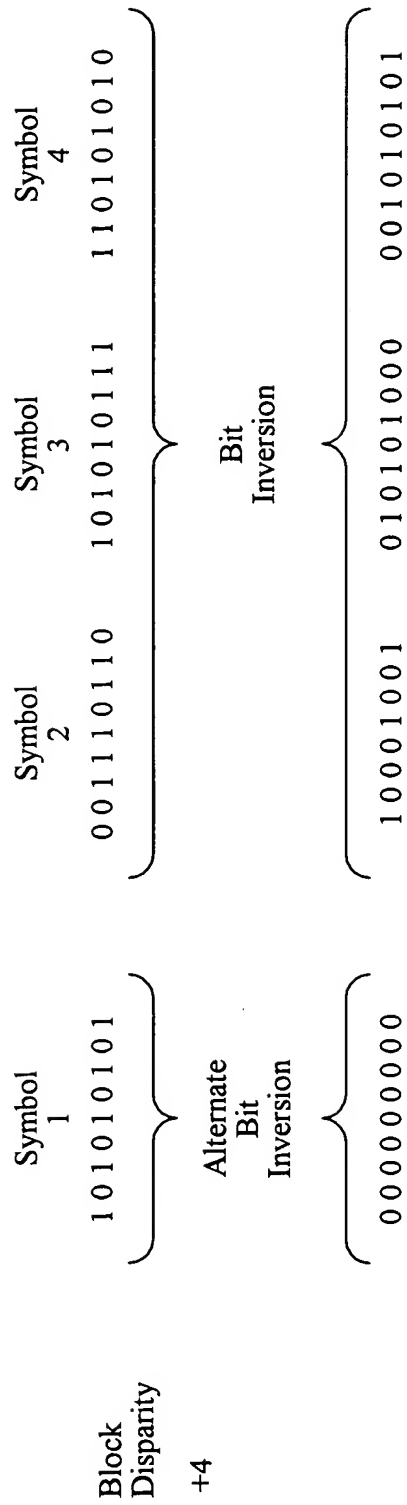


Fig. 21A

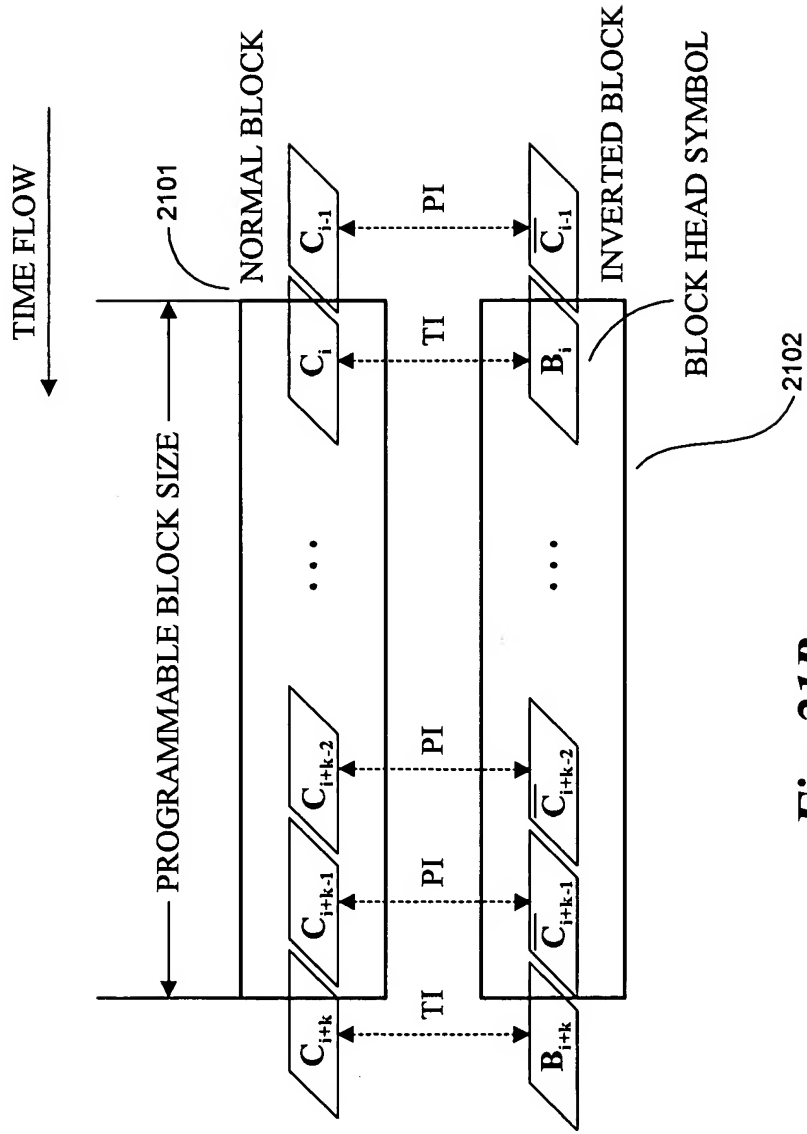


Fig. 21B

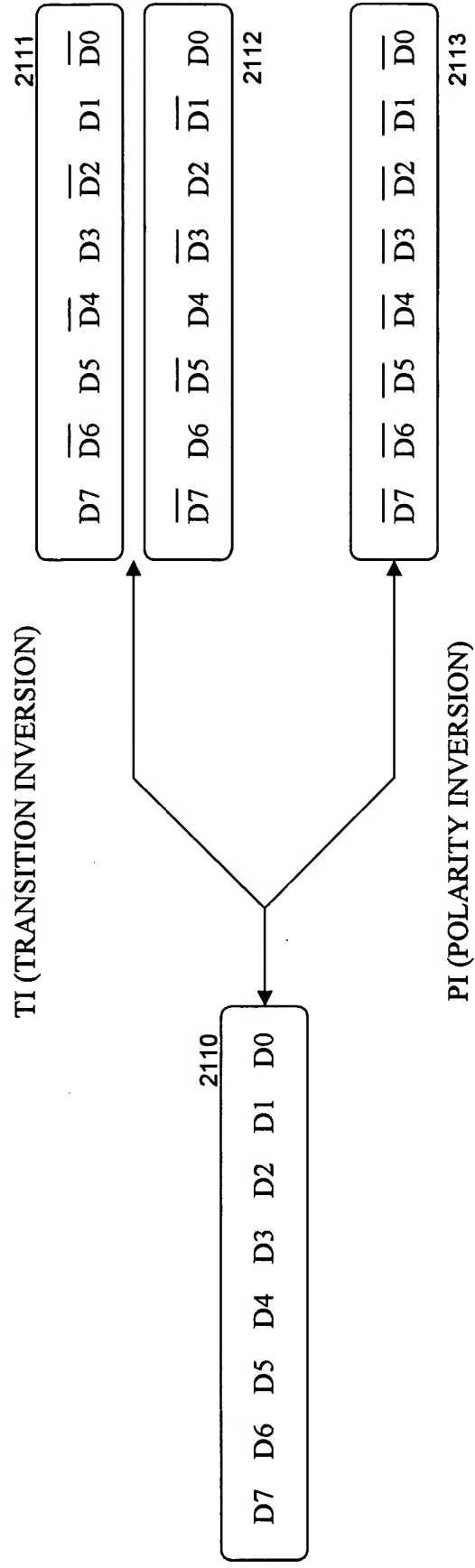


Fig. 21C

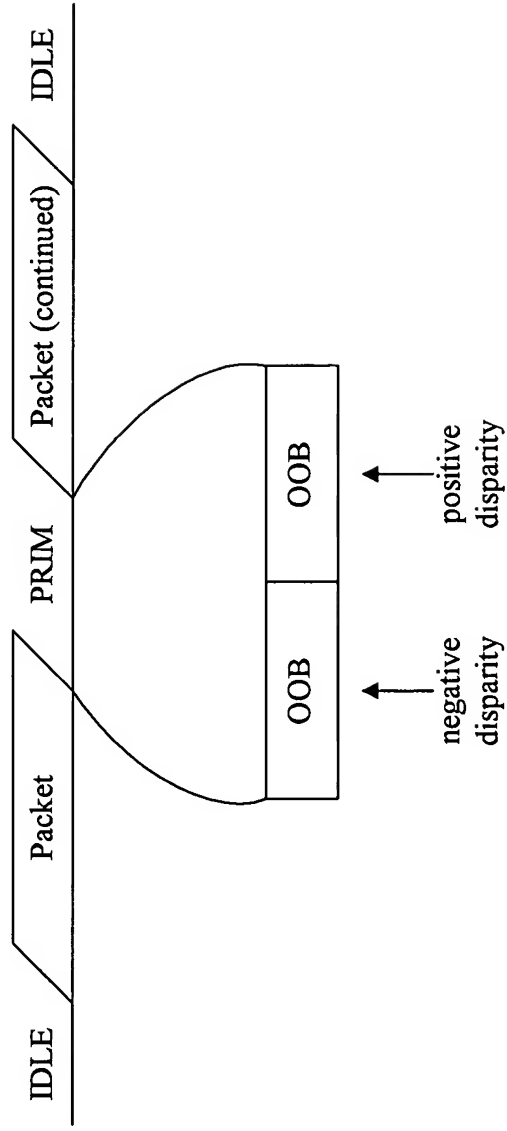


Fig. 22

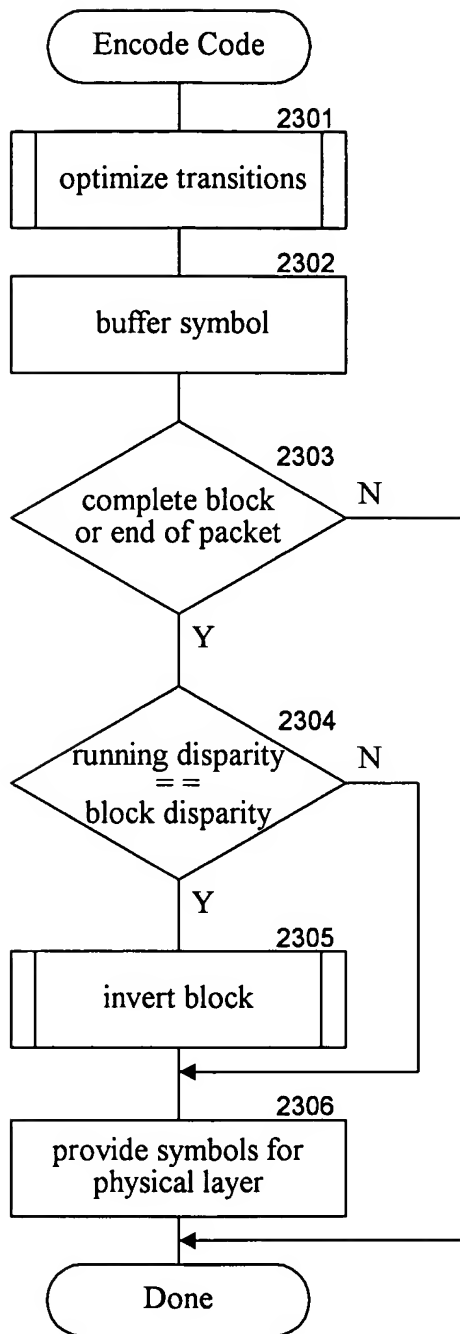


Fig. 23

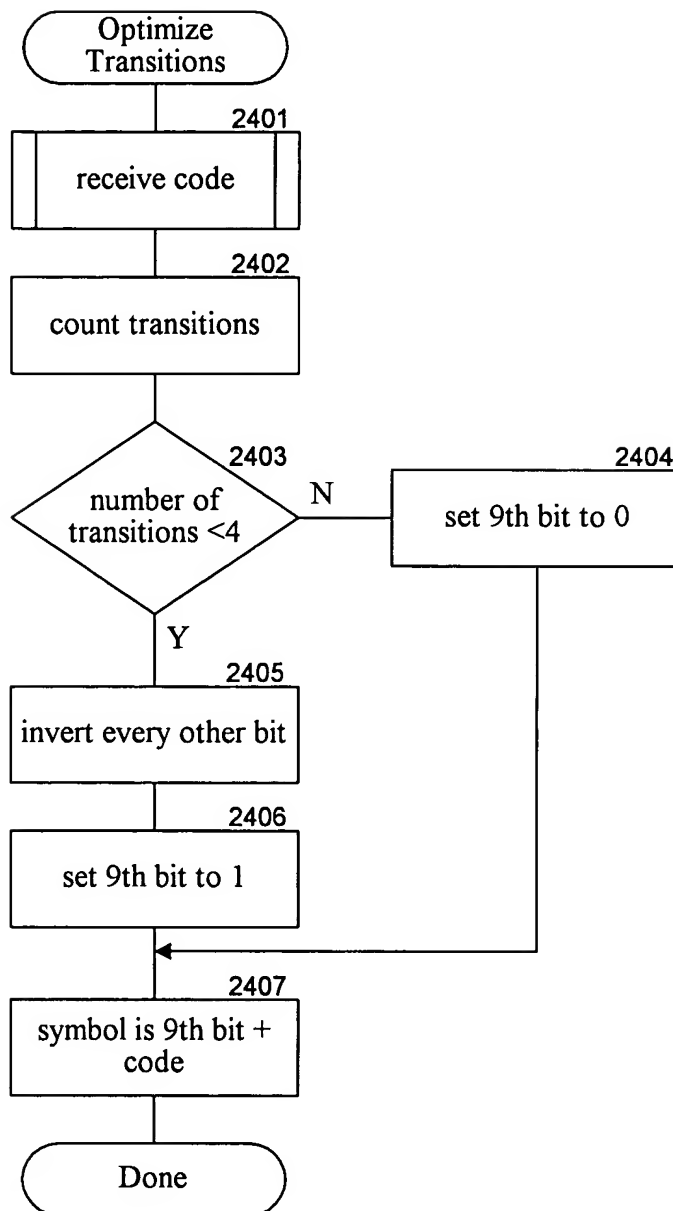


Fig. 24

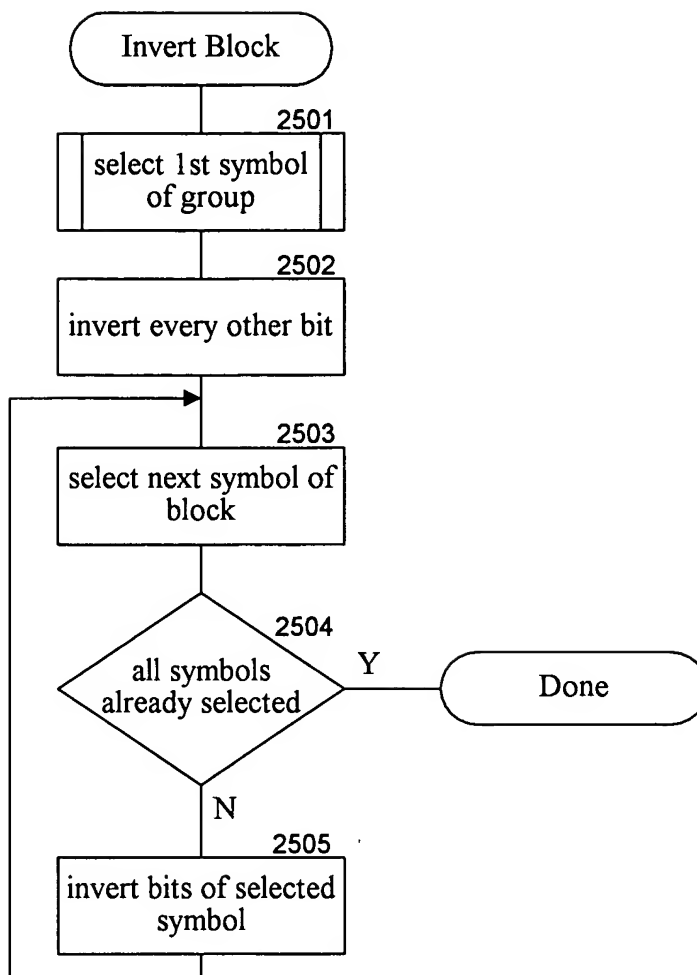
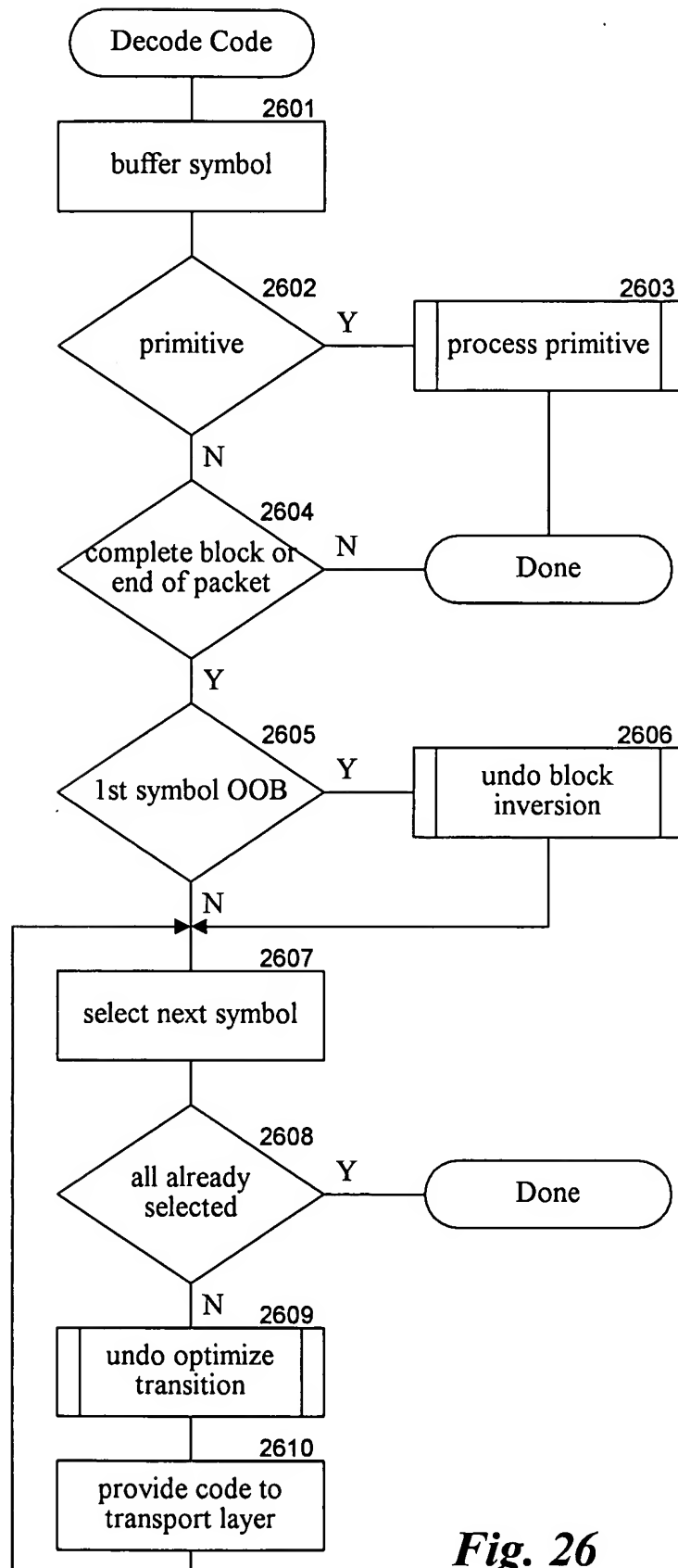


Fig. 25



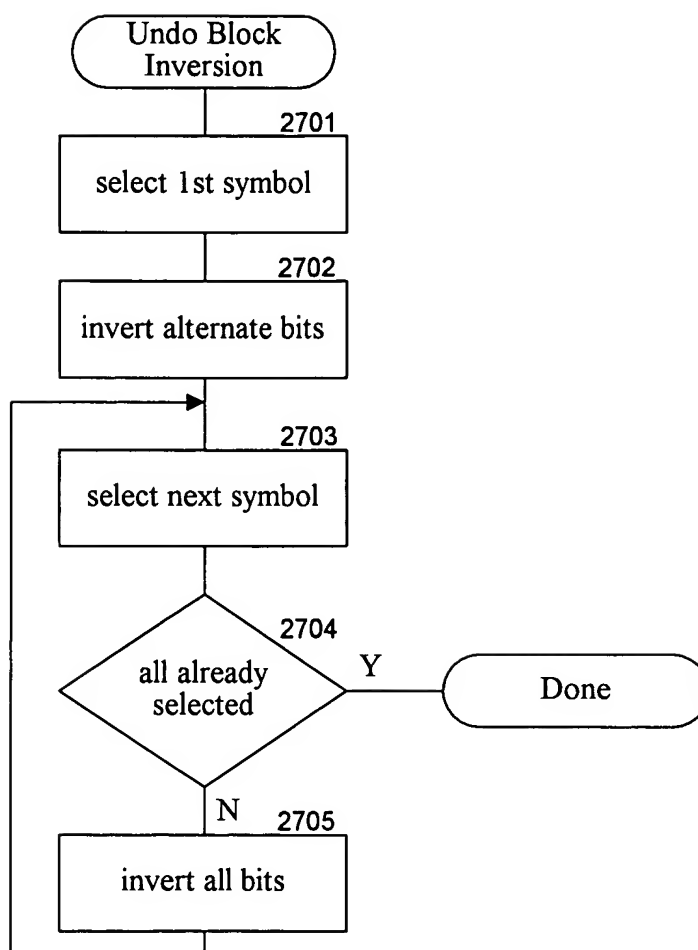


Fig. 27

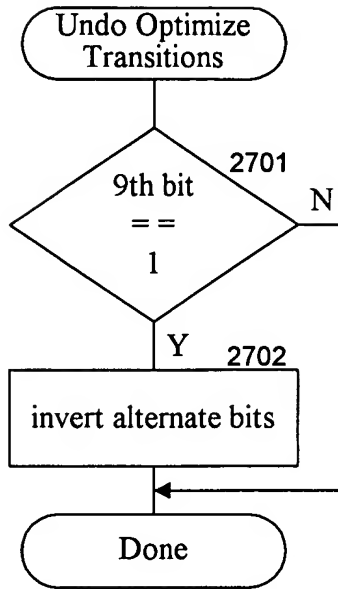


Fig. 28

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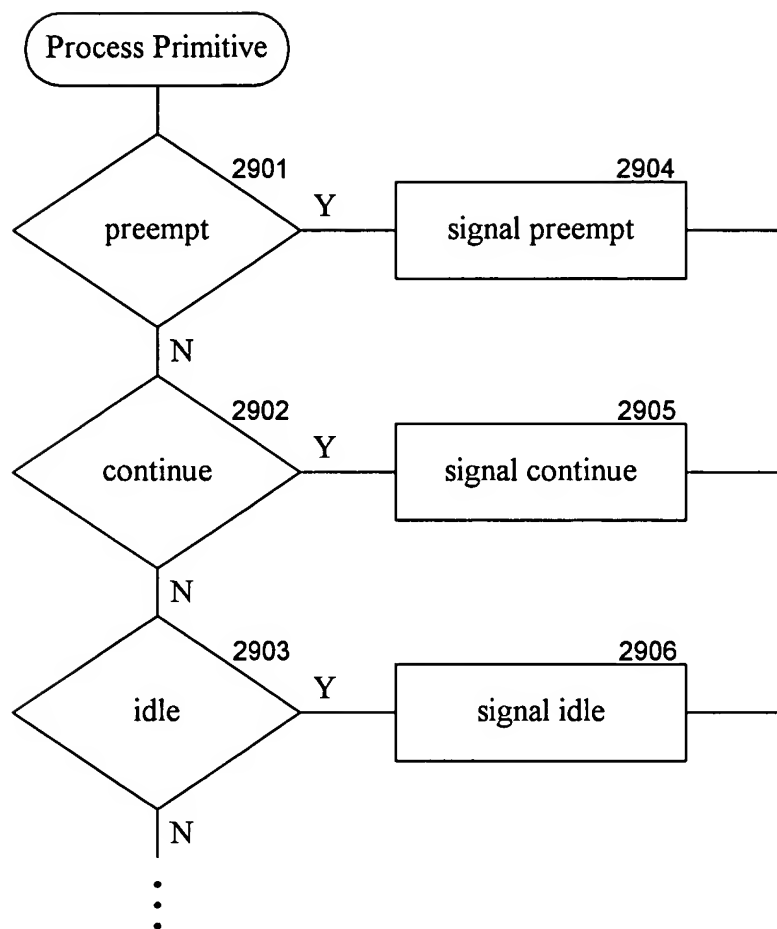


Fig. 29

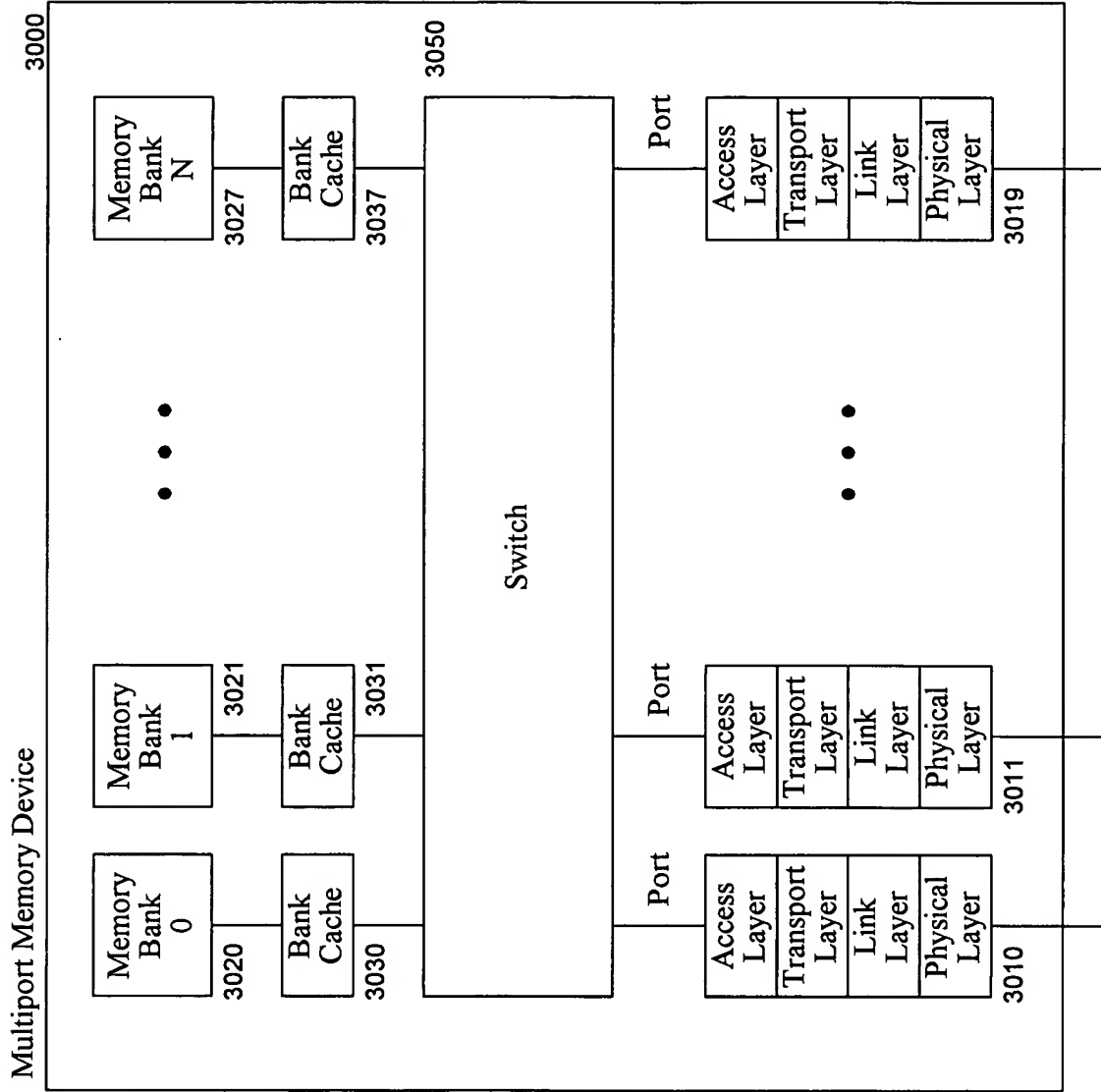


Fig. 30

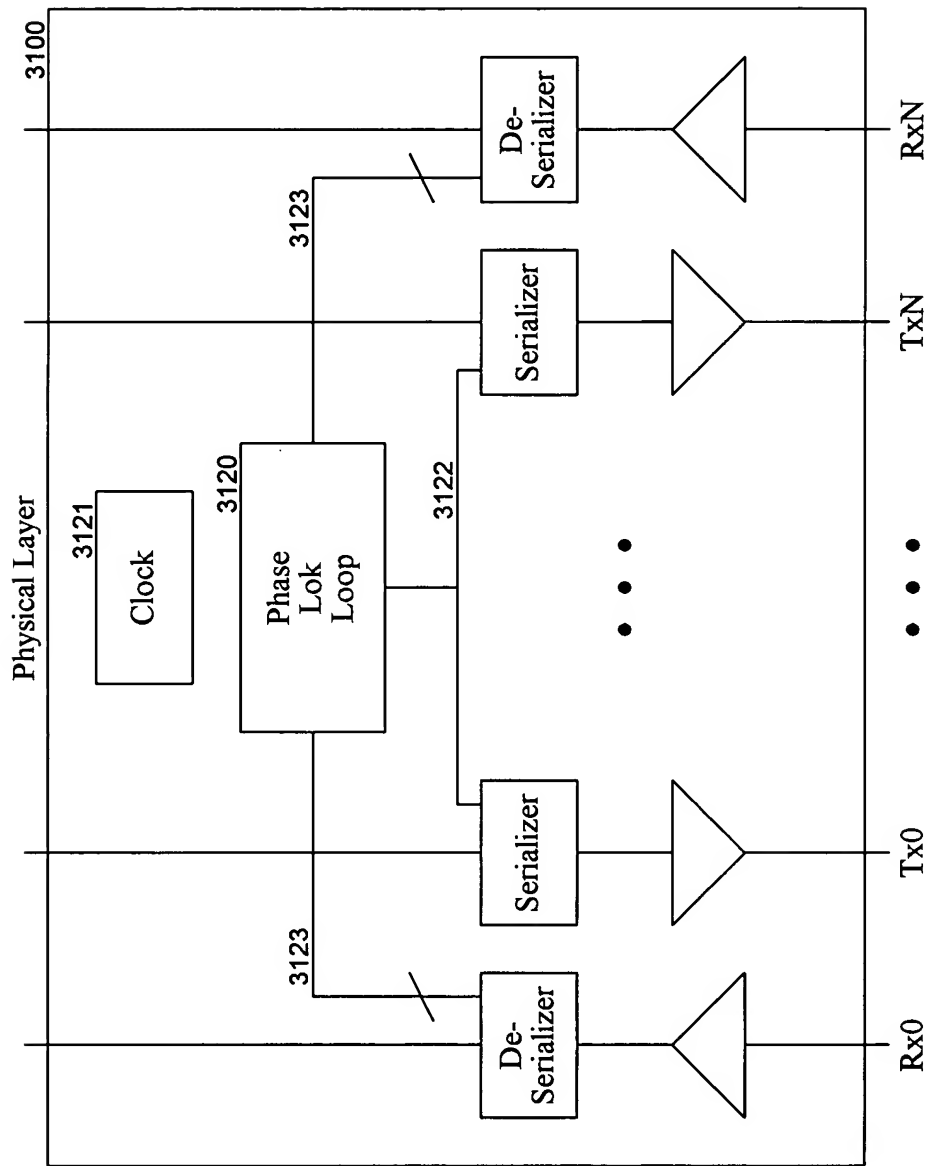


Fig. 31

Input Queue				Output Queue			
3201				3202			
Port	R/W	Address	Data	Valid	Port	Data	
3	R	1000		1	3	11...0	
4	W	4000	10....1	0			
3	W	1000	111...0	0			
3	R	2000		1	3	101...1	
	⋮				⋮		

Fig. 32

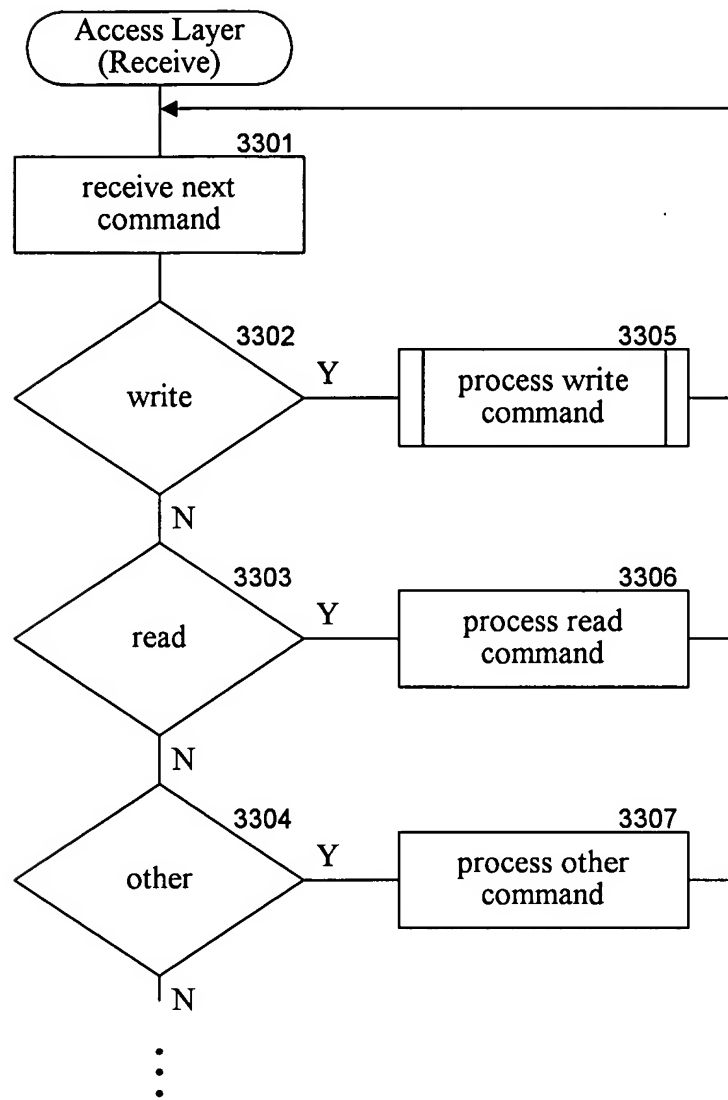


Fig. 33

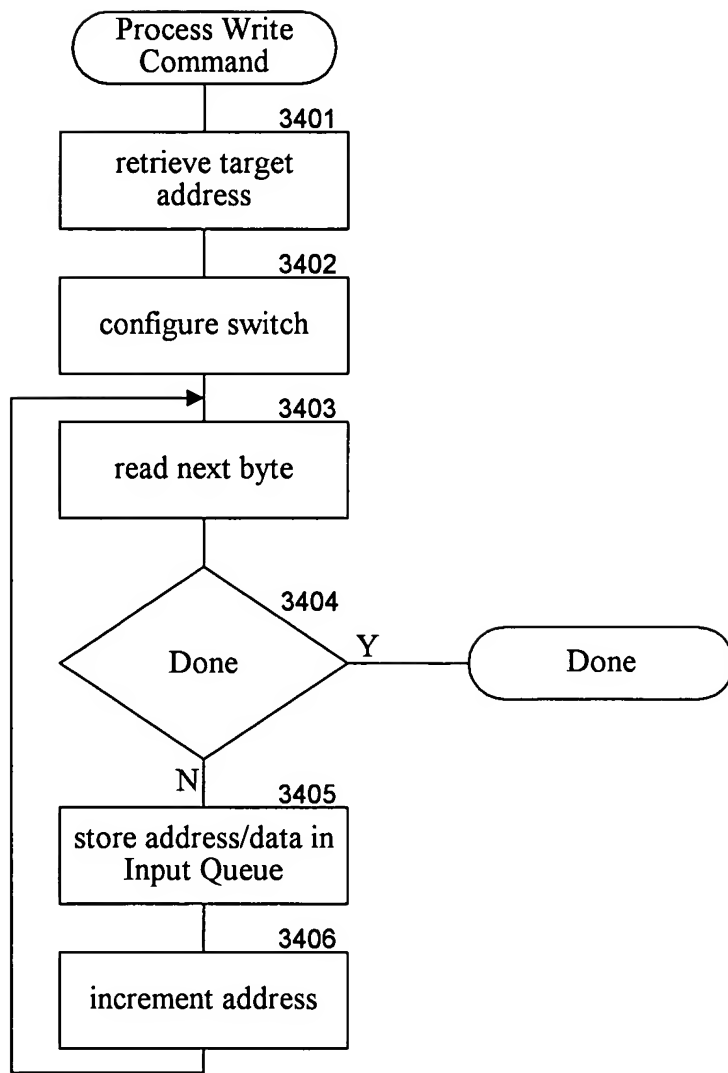


Fig. 34

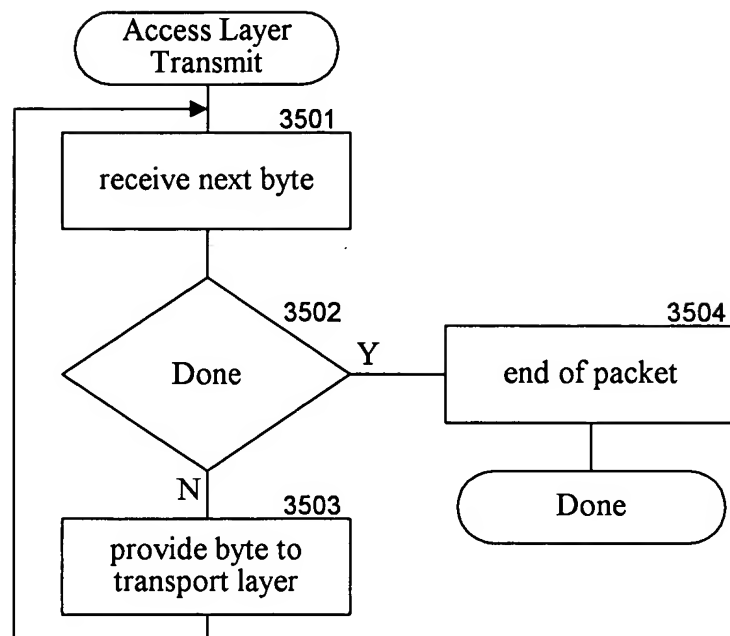


Fig. 35

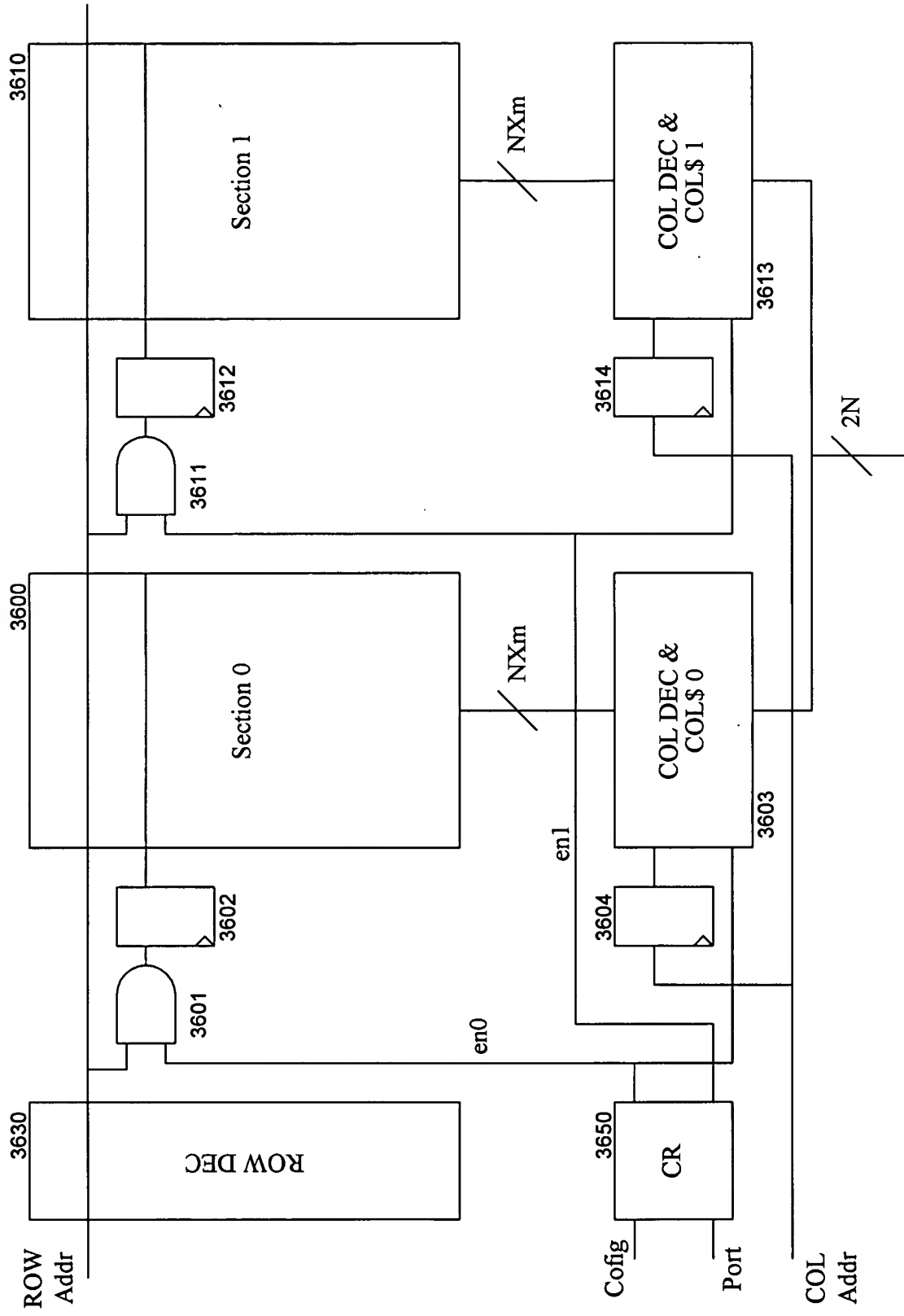


Fig. 36

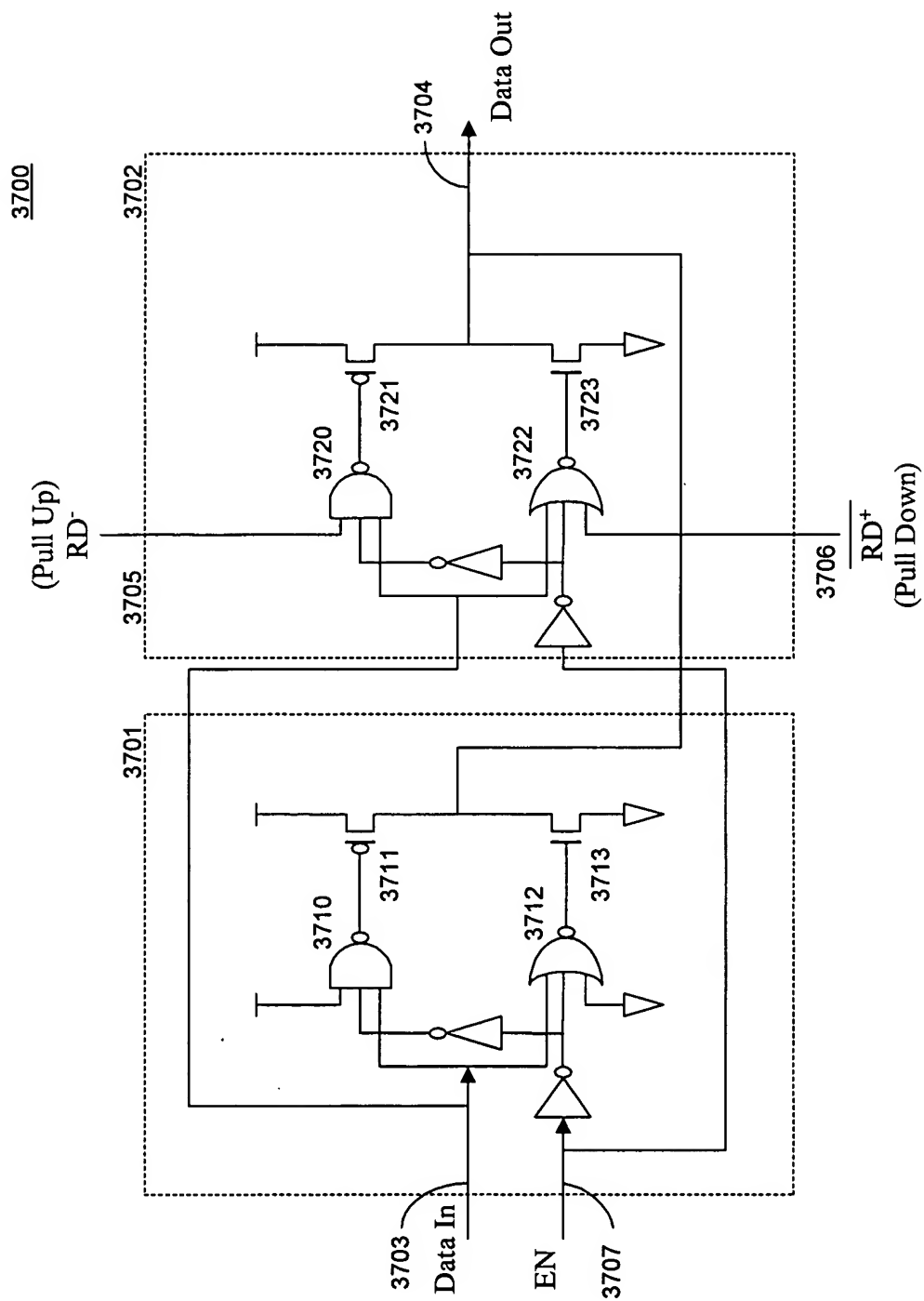


Fig. 37B

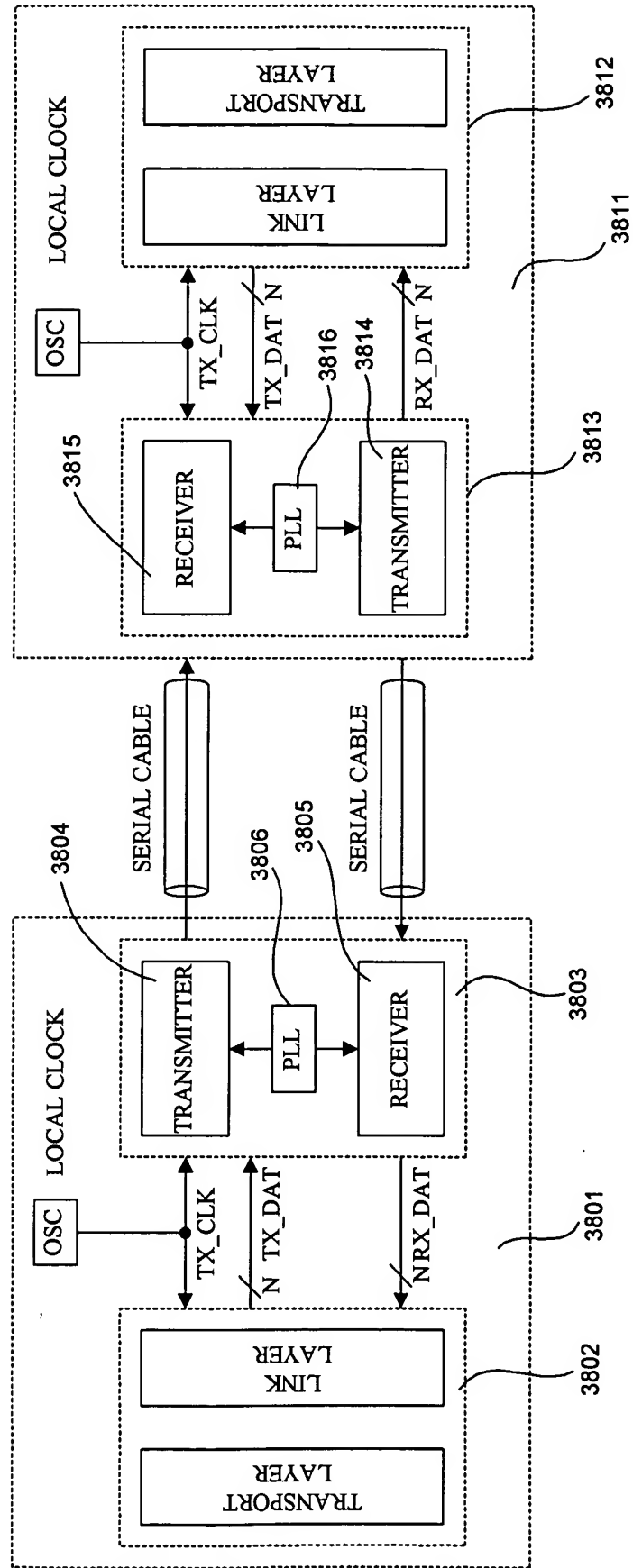


Fig. 38A

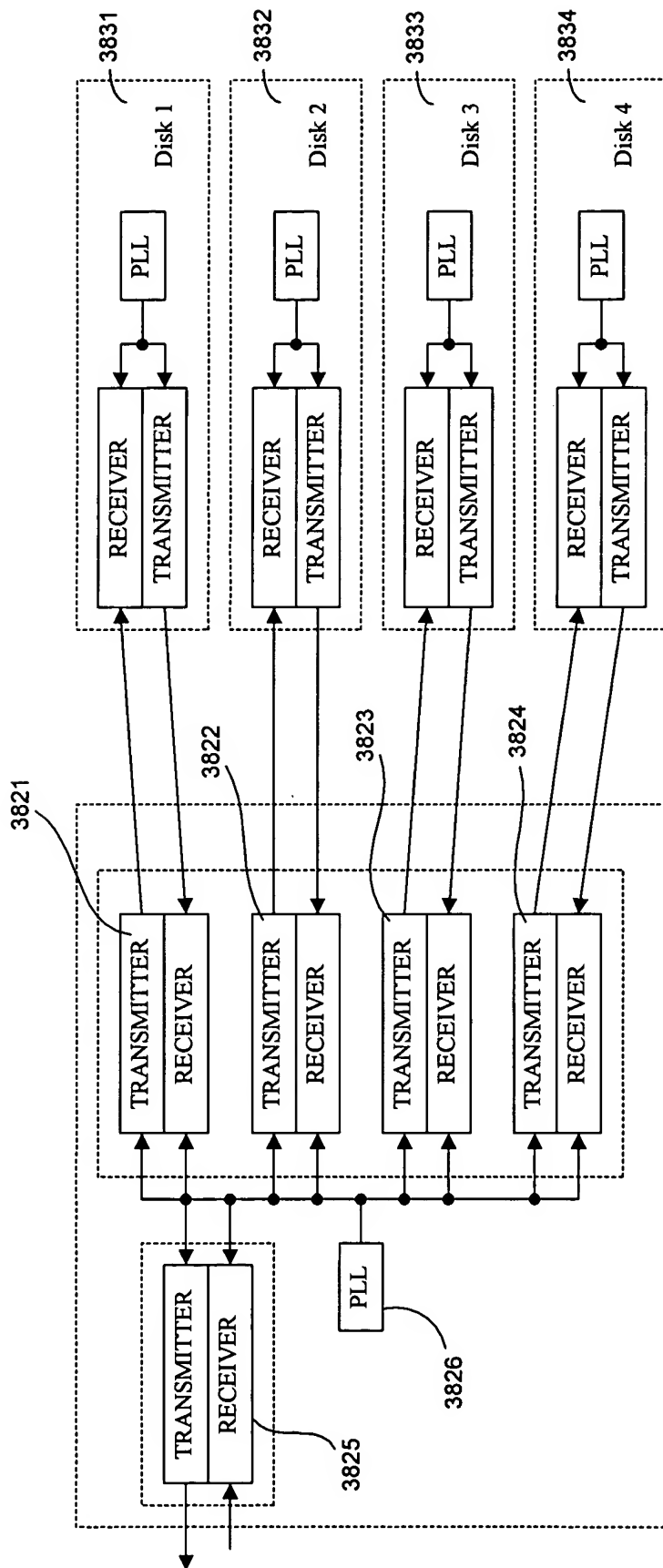


Fig. 38B

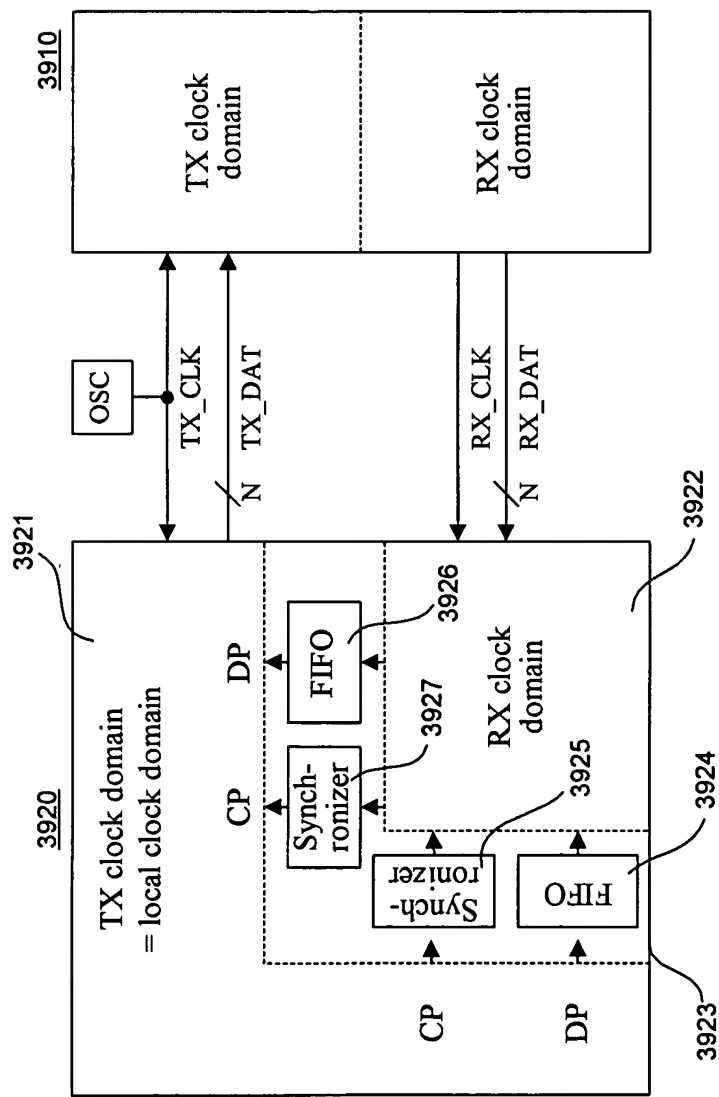


Fig. 39A

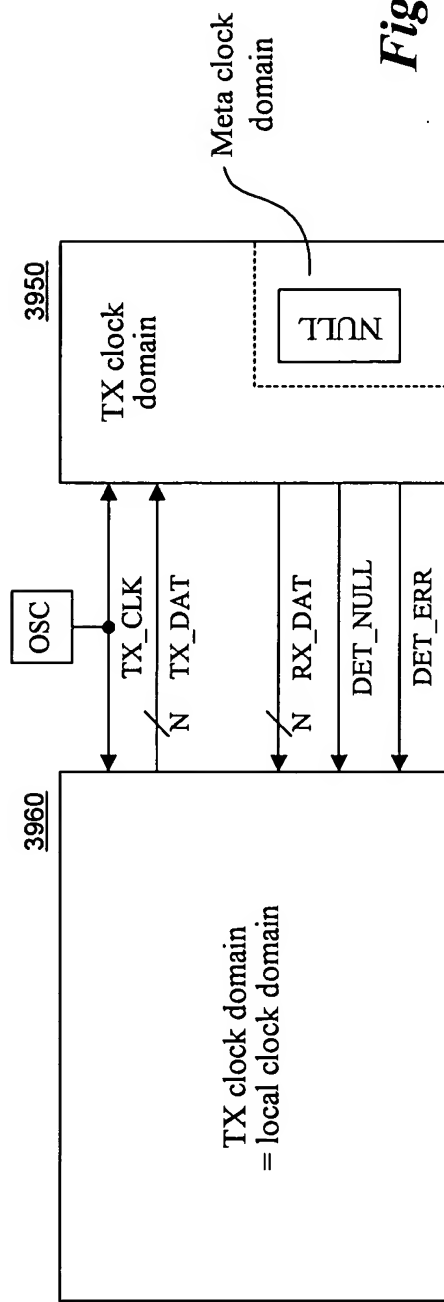


Fig. 39B

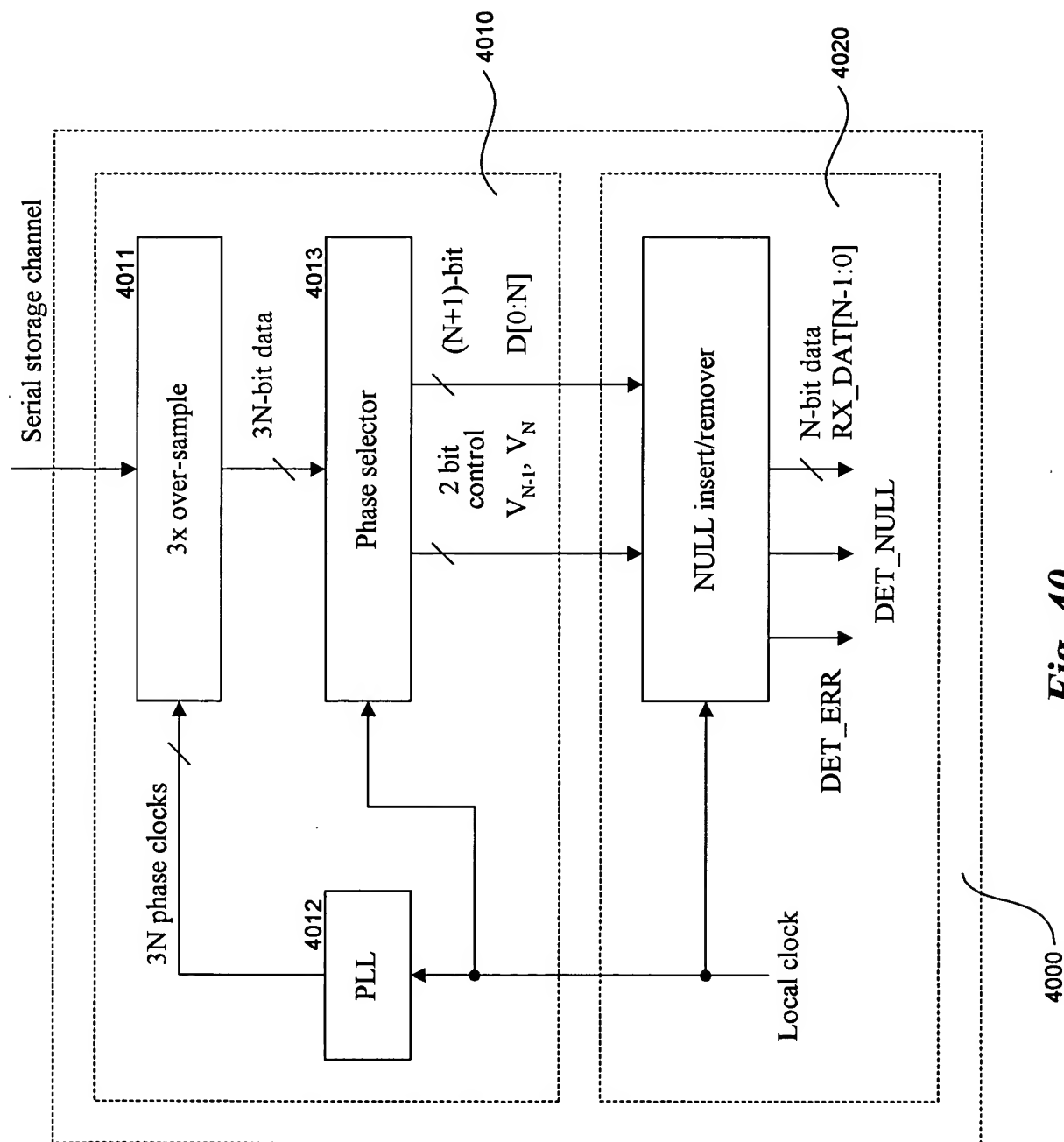


Fig. 40

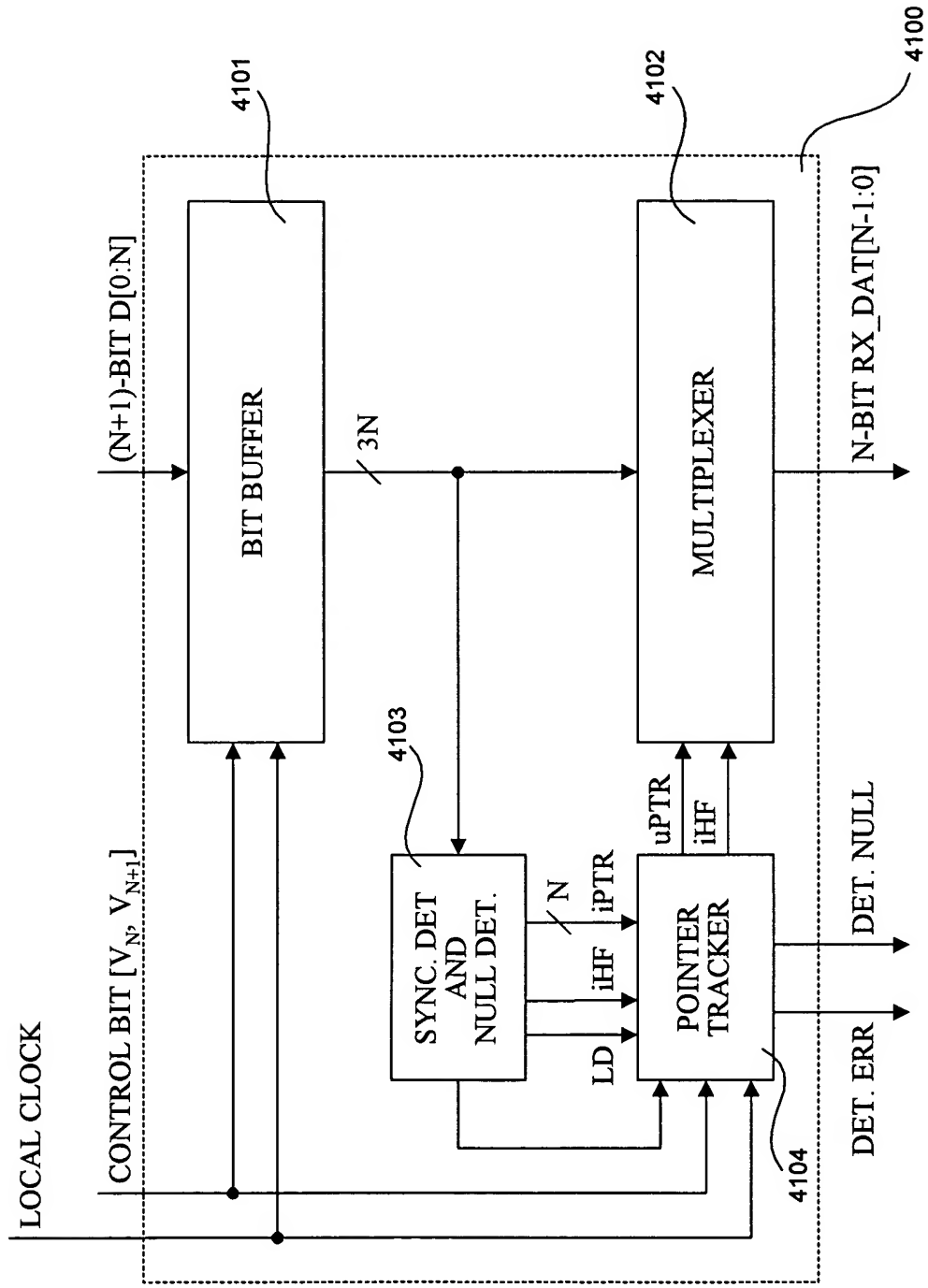


Fig. 41

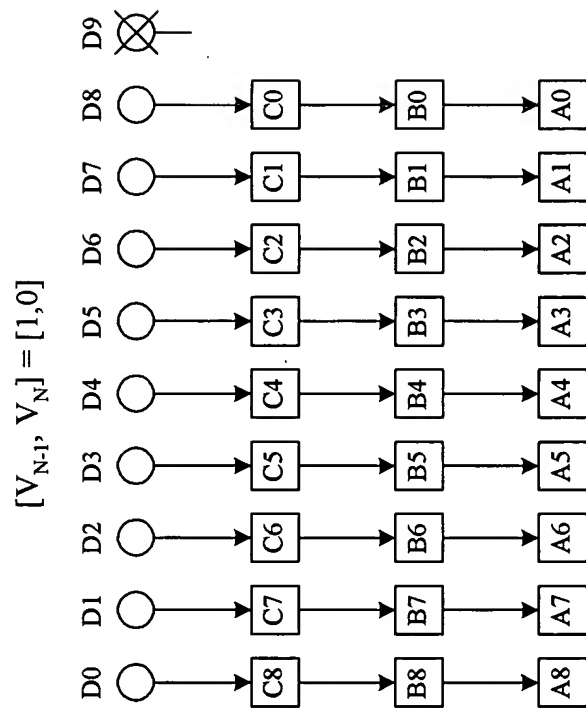


Fig. 42A

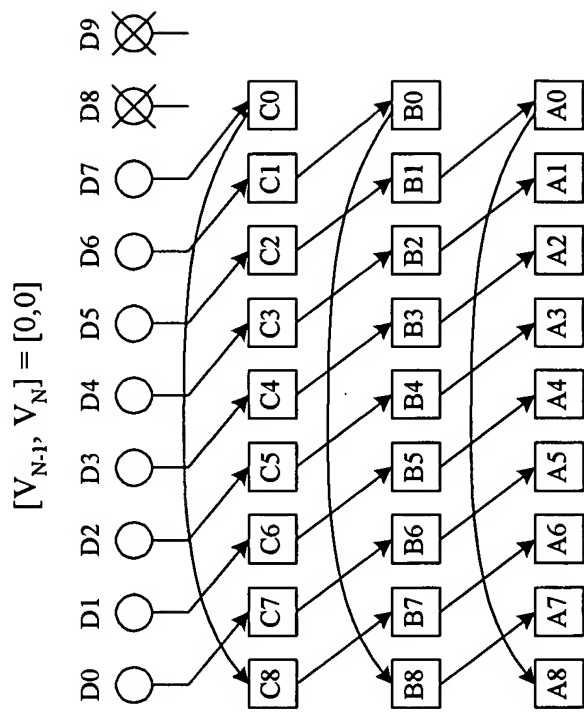


Fig. 42B

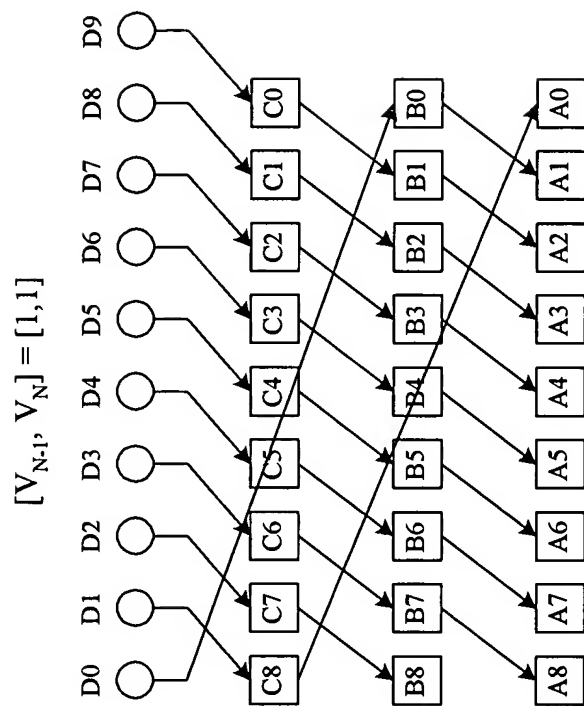


Fig. 42C

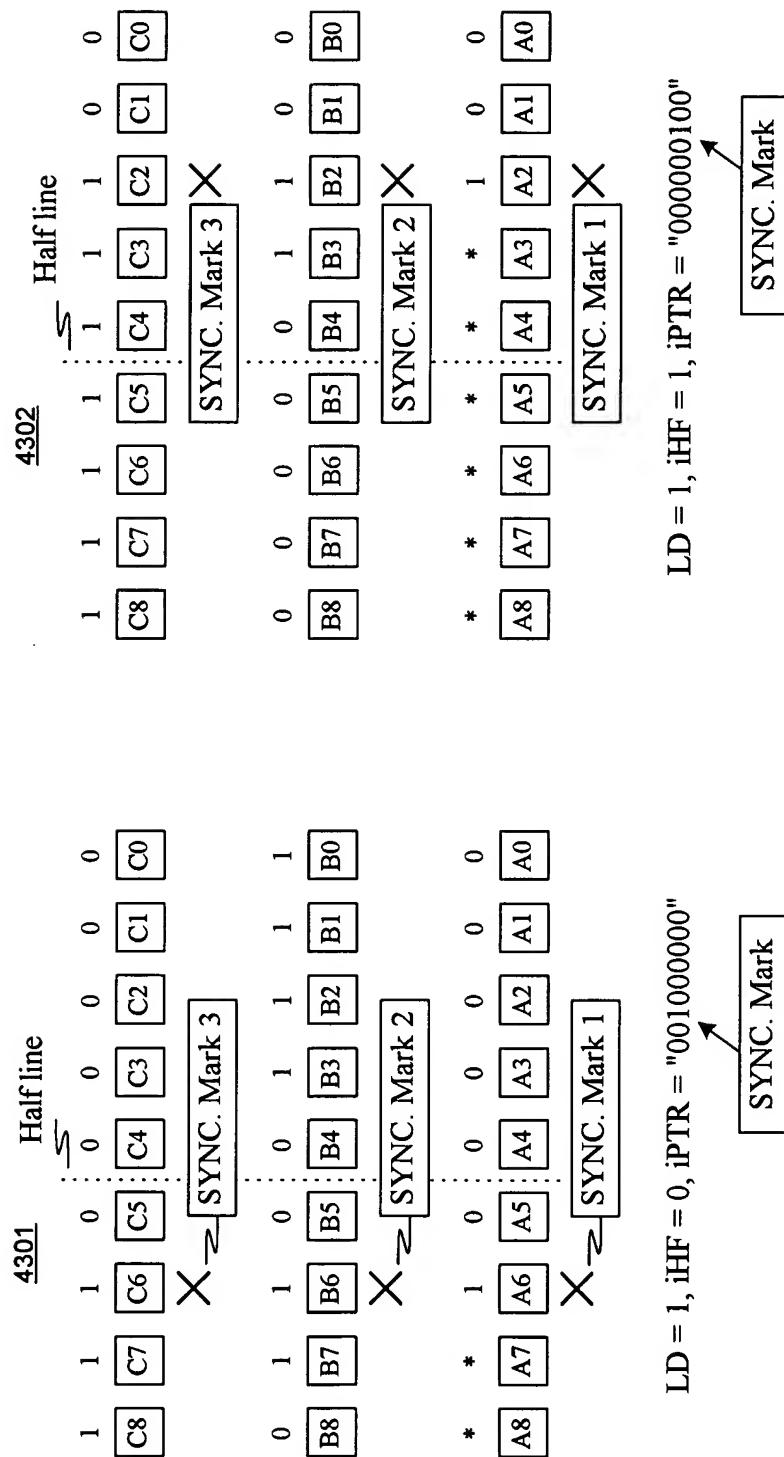
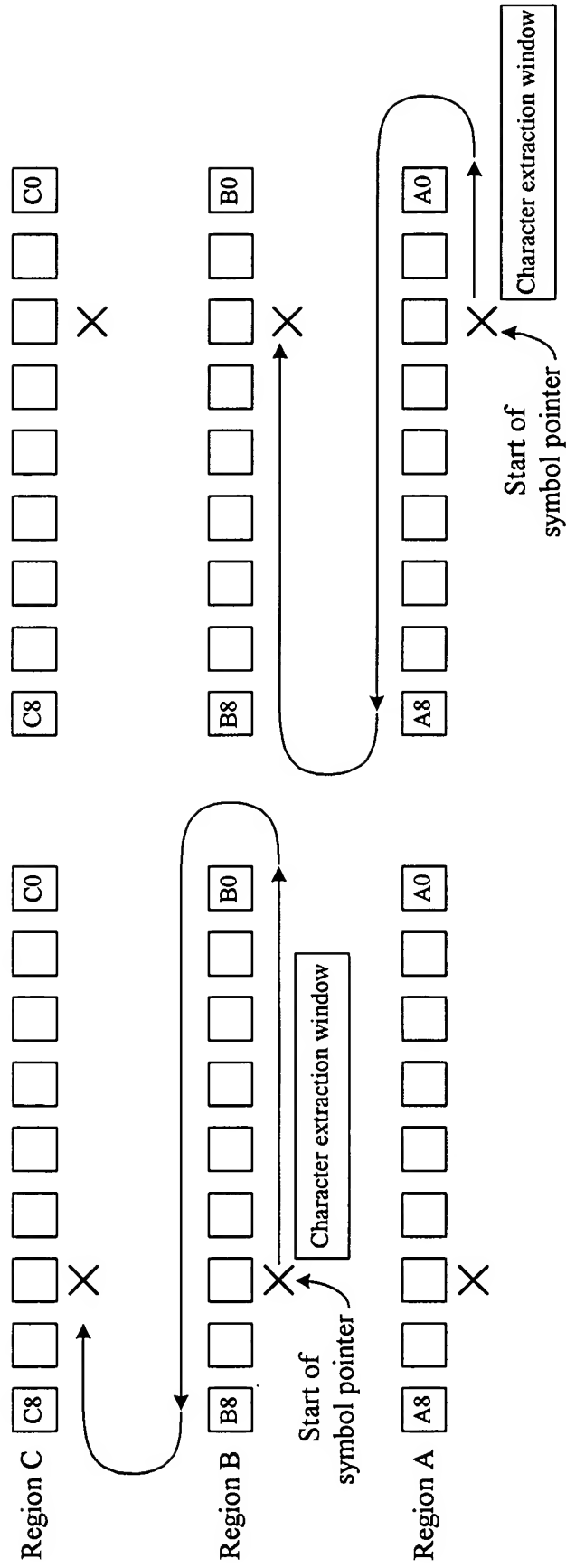


Fig. 43



LD = 1, iHF = 0, iPTR = "001000000"

LD = 1, iHF = 1, iPTR = "000000100"

Fig. 44

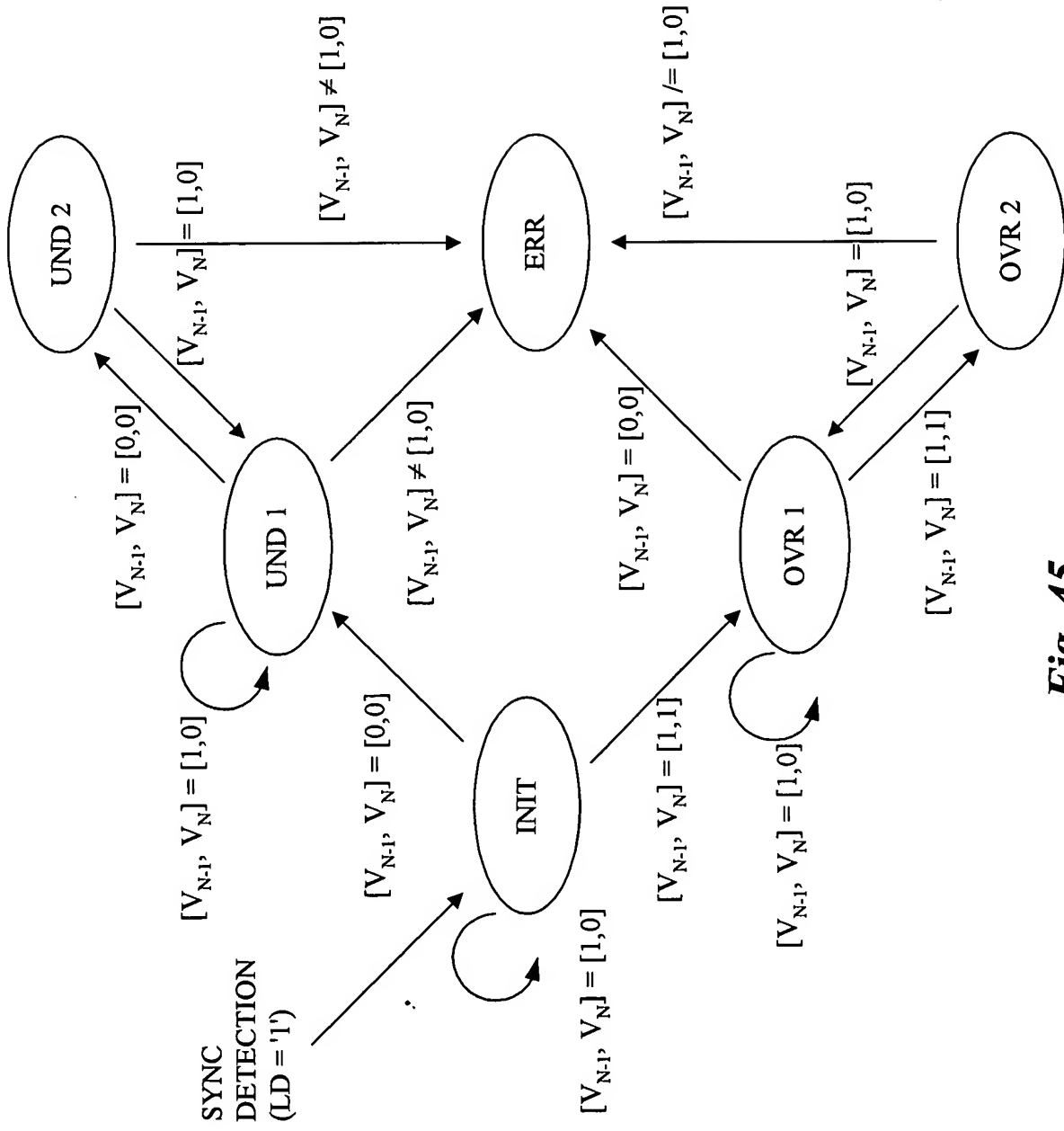


Fig. 45

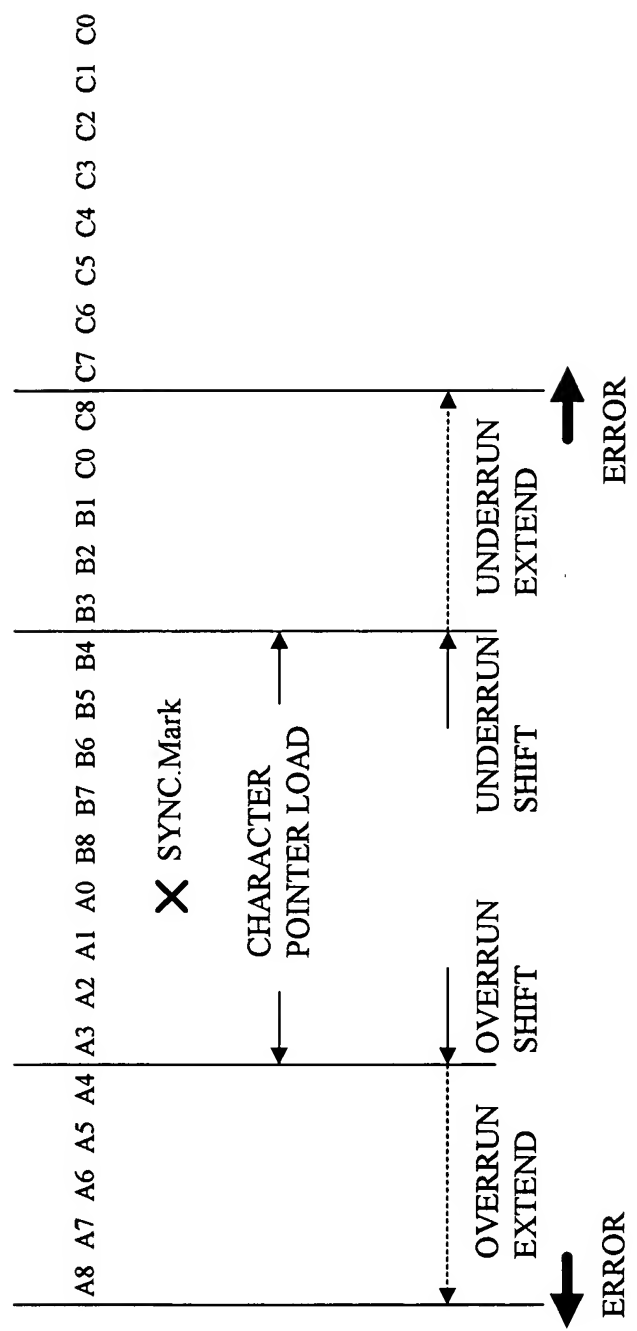


Fig. 46

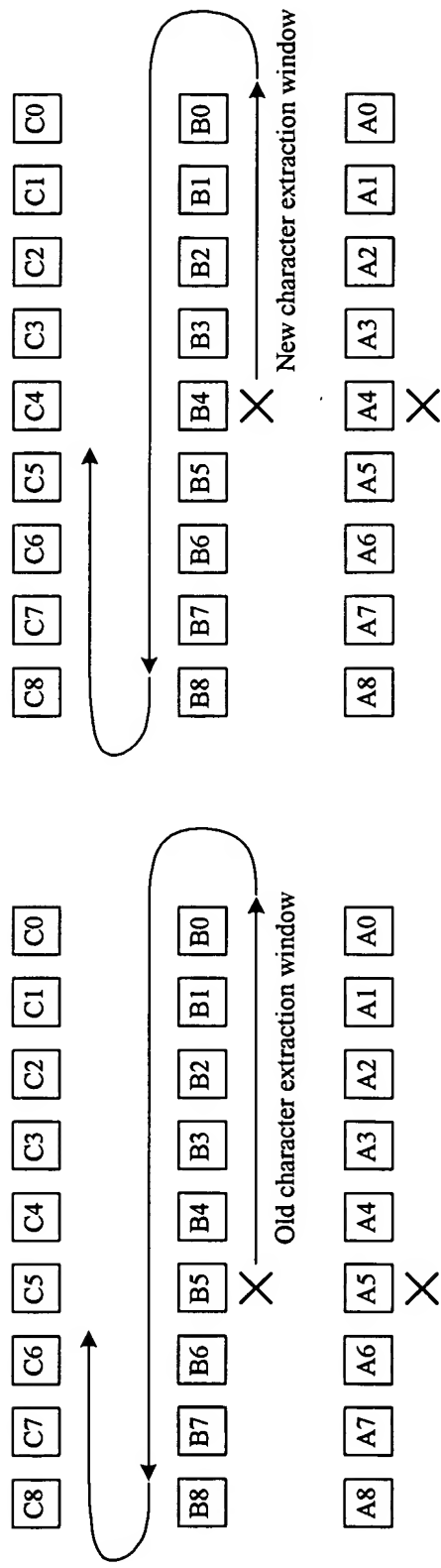


Fig. 47A

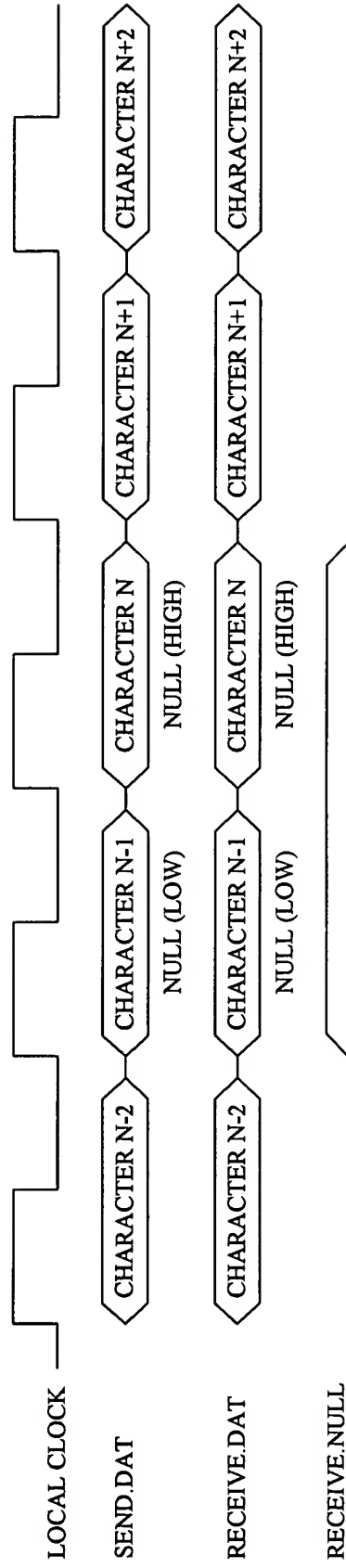


Fig. 47B

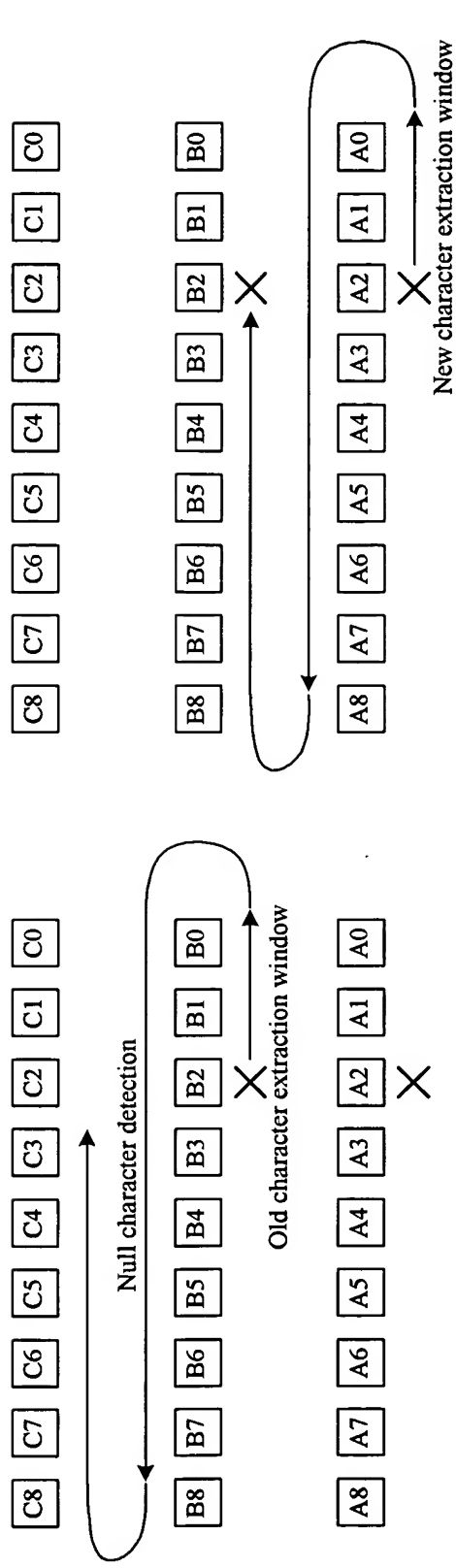


Fig. 48A

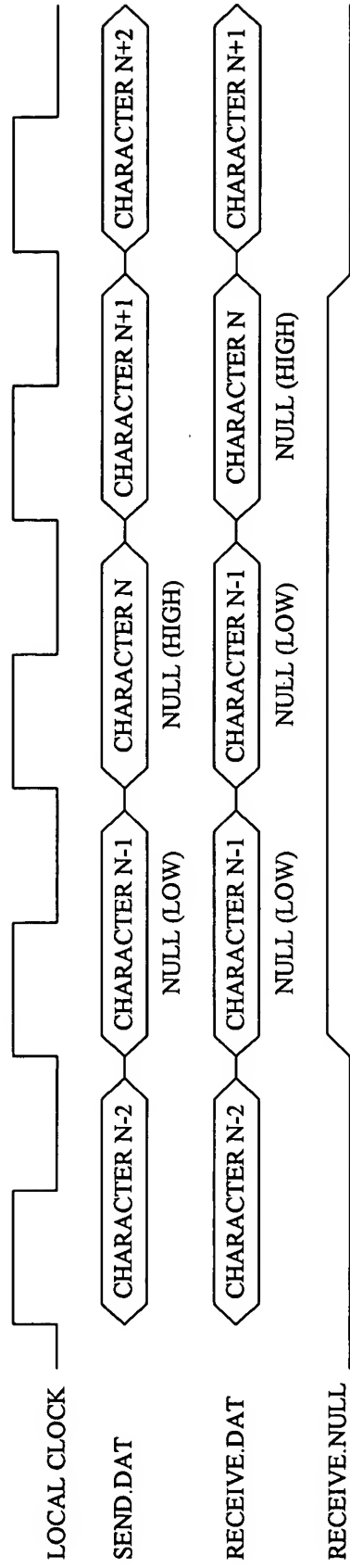


Fig. 48B

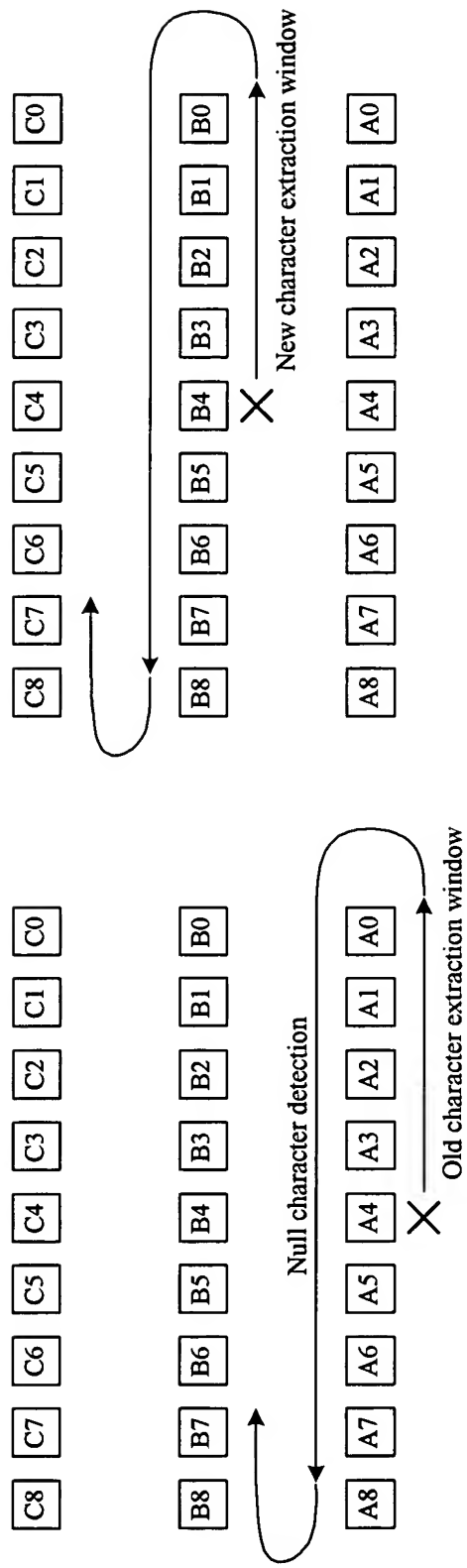


Fig. 49A

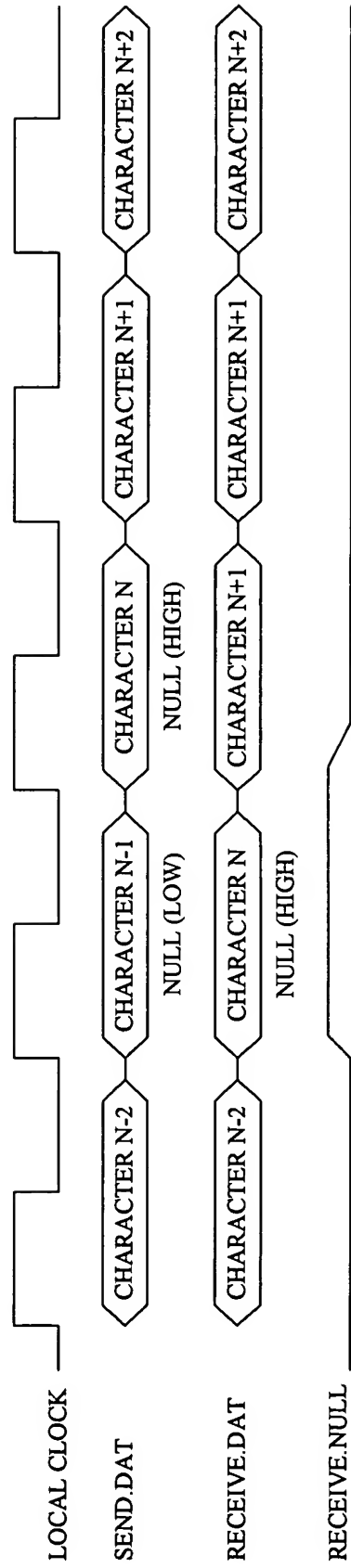


Fig. 49B